How to Design an Integrated Circuit

IC design is detailed and meticulous (i.e. not cheap)
IC fabrication is also not cheap
No user serviceable parts inside – the chip works or it doesn’t
So why do we do this at LBL?
Is IC design really sorcery?

◆ History and Motivation
  – What’s a circuit
  – What’s an integrated circuit
◆ IC design process
◆ Our friend the MOS transistor
◆ Let’s make a chip
◆ Examples
◆ Trends

P. Denes
Engineering Division
Circuit Problem ca. 1750

Charge capacitor \( C \)
Close switch \( S \)
Estimate propagation time through this transmission line
\( N \approx 1000 \)
French physicist Abbe Nollet
Components used:
1000 Carthusian monks
Capacitor based on design from University of Leyden
Resistive contact to C
Circuit Layout

- Simultaneous jumping of monks $\rightarrow$ “electricity is fast”
- Circuit composed of well-defined, discrete parts connected together
- (Circuit dimensions are a bit large)

~900 feet
Fast Forward → 1906

Grid modulates conduction

- Can be used for analog applications
- Can also be used for digital applications
ENIAC – 1945, U. Penn.

Designed to calculate ballistic ordnance firing tables
Electronic Numerical Integrator And Computer

But then, some work at a famous industrial lab changed everything

Its thirty separate units, plus power supply and forced-air cooling, weighed over thirty tons. Its 19,000 vacuum tubes, 1,500 relays, and hundreds of thousands of resistors, capacitors, and inductors consumed almost 200 kilowatts of electrical power.
IBM 701 -1952

16 kHz cycle
2k words fast storage
1\textsuperscript{st} computer for scientific work

Modular circuit assemblies of components
The solution?

Point contact transistor

Thin razor cut

Revolutionary Amplifier
The CRYSTAL TRIODE
Almost

- Point contact transistor is a surface effect device (and surfaces are easy to contaminate – not to mention paper clips can be mechanically unstable)
- Schottky contacts, rather than pn junctions
- Shockley junction transistor (1949)

![Diagram of a transistor with labels: Emitter (E), Collector (C), Base (B), p, n, p, and Ge.]

Although the point contact transistor did live for a while
CDC 1604/160 - 1960

160 kHz cycle
32k words fast storage

Modular circuit assemblies of components

The first desktop (literally)
Integrated Circuits - 1958

Jack Kilby
Ge
(1 transistor)

Texas Instruments
(Patent)

Robert Noyce
Si
(2 transistors)

Fairchild
(Patent)

Legal wrangles Resolved in mid-60’s
Early Circuits – Planar Bipolar Process

p+ substrate
Early Circuits – Planar Bipolar Process

- high resistivity p- epitaxial layer
- p+ substrate
grow SiO$_2$ and open base window

high resistivity p- epitaxial layer

p+ substrate
Early Circuits – Planar Bipolar Process

n implant

high resistivity p- epitaxial layer

p+ substrate
Early Circuits – Planar Bipolar Process

- p+ substrate
- high resistivity p- epitaxial layer
- p+ implant
- n+

p+ substrate
Early Circuits – Planar Bipolar Process

Contacts/Metal

p+ substrate

high resistivity p- epitaxial layer
Bipolar Junction vs. Insulated Gate Transistors

\[ I_C \sim \beta I_B \]
\[ I_B \sim \exp(V_{BE}/kT) \]

\[ I_D \sim (V_{GS} - V_T)^2 \quad V_{GS} > V_T \]
\[ I_D \sim 0 \quad V_{GS} < V_T \]

1st MOS on Si - 1960
MOS and CMOS take over

- Early circuits were mostly bipolar (especially analog)
- MOS took hold for memory
- CMOS invented in 1963, but took off (once fabrication became good enough) in the 80’s
The first single chip CPU was the Intel 4004, a 4-bit processor meant for a calculator. It processed data in 4 bits, but its instructions were 8 bits long. Program and Data memory were separate, 1K data memory and a 12-bit PC for 4K program memory (in the form of a 4 level stack, used for CALL and RET instructions). There were also sixteen 4-bit (or eight 8-bit) general purpose registers.

The 4004 had 46 instructions, using only 2,300 transistors in a 16-pin DIP. It ran at a clock rate of 740kHz (eight clock cycles per CPU cycle of 10.8 microseconds) - the original goal was 1MHz, to allow it to compute BCD arithmetic as fast (per digit) as a 1960's era IBM 1620.
**Process** – the complete fabrication process which produces the integrated circuits. It includes photolithographic mask preparation, wafer preparation and processing, etc. The *process* defines for the designer what kinds of devices are available and what their performance characteristics should be.

**Feature size (or line width)** – the smallest dimension which can be reliably lithographed. So a “1 µm CMOS process” contains N- and P-channel MOS transistors with 1 µm minimum feature size.
ENIAC – 50th Anniversary Edition

Size: 7.44mm x 5.29mm; 174,569 transistors; 0.5 um CMOS technology (triple metal layer).

30 mg vs 30 tons
Digital Standard Cells

- Predefined logic gates ("cells") - Circuit composed of well-defined, discrete parts connected together
- write a description (program) of the logic functions
- synthesize the design (using the library)
- place and route the design
For example
But This Is Not What We Do

We do mixed-mode design - analog functions, supported by digital logic.

The analog functions are full custom: design the circuit at the transistor level, and design/optimize each transistor for the given function. This is not assembling a collection of pre-defined modules.

Timeout - Glossary

Full custom design means that we draw each transistor. What we can adjust are the width (W) and length (L) of the channel. For a given process, the transconductance ($\partial I/\partial V$) and capacitance depend on W, L and the process parameters.
Why do we do this?

High rate fixed target experiments in the ’80s (NA11, E706, …) needing finer granularity (to reduce occupancy)

Particle Tracking Detectors

Higher density of electronics and interconnect required

5x5 cm$^2$ Si strips
What we do

- Design custom ICs, typically in support of lab programs
- Generally, these ICs have many channels and are connected to some sort of sensor, transducer, … at the front-end, do some sort of signal acquisition/processing, and send information, usually digital, off the back end of the chip

- We conceptualize the design, implement it electrically and produce the data needed to prepare the masks
- We *don’t* actually fabricate the ICs – we use commercial IC processes

Analog FE “Conversion” Digital BE
Commercial Processes

- Mask sets for modern technologies are very expensive (so we don’t work at the cutting edge)
- One wants to try ideas out first anyway, so we use “Multi-project” services (brokers, who assemble many people’s projects onto one run)
- So our technology choices are limited
Large R&D Investment

WW SEMICONDUCTOR INDUSTRY REVENUE (3 Year Avg)

2003 investment ~$14B (17% of sales). Recently, investment ~12-15% of sales...
Steps in the IC Design Process

1→0?
0→1?

Conceptual Design
- Negotiate the specs

Initial Behavioral Design
- No transistors yet
- Technology selection

Schematic Design & Simulation
- Circuit solutions
- Transistor design

Layout and Verification
- Optimization
- DRC, LVS
- Fight the tools!

Post-layout Simulation
- parasitic extraction
- Fight the tools!

Tape out!
Let’s Make A Chip

This will be a pretty banal example to fit within the time of this talk

For a made-up application, we have a high-output-impedance sensor that needs a buffer amplifier. Specifications:
- Drive an output load of 1 pF in less than 10 ns
- Use no more than 1 mW
- Be precise to >6 bits

\[CL = 10\text{pF} \quad \infty \Omega \quad \leq 10 \text{ns}\]
Our Friend the MOS Transistor

[Diagram of MOS Transistor with labels: G = Gate, S = Source, D = Drain,Channel L, Channel W, TOX, T_{ox}, Bulk, Gate Oxide]
Design

Current Mirror

Same $V_{GS}$
Same current
Design

Current Mirror

Same $V_{GS}$
Same current

$I_{IN}$ $I_{OUT}$
Design

Current Mirror

Same $V_{GS}$
Same current
Hand Calculation

$\mu = 0.03 \text{ m}^2/\text{V} \cdot \text{s}$  
$T_{ox} = 7.1 \text{ nm}$

$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{T_{ox}} = 0.0048 \text{ F/m}^2$

1 mW $\Rightarrow$ 400 $\mu$A

$g_m = \frac{\partial I}{\partial V_{gs}} = \sqrt{\mu C_{ox} \frac{W}{L}}$

$= 2 \text{ mA/V for } \frac{W}{L} \sim 140$

Check the calculation with simulation
Simulation

**Netlist**

MS2 D1 D1 VDD VDD PCH L=1U W=80U M=1
C1 OUT GROUND 1P
V3 N$617 GROUND DC 0V AC 1 0
V2 INP N$617 PULSE ( 1 1.5 50N 1NS 1NS 1 2 )
I1 VDD N$207 DC 0.25MA
MN4 N$207 N$207 GROUND GROUND NCH L=1U W=20U M=1
MN3 OUT OUT S1 GROUND NCH L=0.28U W=39U M=1
MN2 D1 INP S1 GROUND NCH L=0.28U W=39U M=1
MS1 OUT D1 VDD VDD PCH L=1U W=80U M=1
MN1 S1 N$207 GROUND GROUND NCH L=1U W=20U M=1
V1 VDD GROUND DC 2.5V

**Choice of model**

\[ I = \frac{\mu C_{OX} W}{2} \left( V_{GS} - V_T \right)^2 \]

**Process parameters**

\[ \mu = 0.03 \text{ m}^2/\text{V} \]

\[ T_{OX} = 7.1 \text{ nm} \]

\[ C_{OX} = \frac{\varepsilon_{OX} \varepsilon_0}{T_{OX}} = 0.0048 \text{ F/m}^2 \]
How Did We Do?

Response to a 1 → 1.5V step
2nd Order Effects are Critical in IC Design

◆ $g_m$ – not too bad, hand calculation $\rightarrow 2 \text{ mA/V}$, simulation $\rightarrow 1.86 \text{ mA/V}$

◆ $R_{DS}$ – not so good, hand calculation $\rightarrow \infty \Omega$, simulation $\rightarrow 24 \text{ k}\Omega$
  – Channel length modulation: $I_{DS} \rightarrow I_{DS}(1 + \lambda V_{DS})$ so $R = 1/\lambda I_{DS}$

◆ DC gain – not so good, hand calculation $\rightarrow \infty$, actual value is $A_V = g_m R_{DS} = 1.86 \text{ mA/V} \times 24 \text{ k}\Omega \sim 50 \Rightarrow$ offset of 1-2%

◆ OK – so now, I understand everything, right?
Modern Devices are more Complicated

Simple model

Modern Reality
2nd Order Effects may be 1st Order for the Design

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) \quad \frac{1}{n kT / q} \quad \frac{I_D}{C_G}
\]

For a preamp, maximize \( g_m / C_G \)

Sub-threshold slope \( 1 \ln kT / q \)

Junction Leakage

Strong inversion model

Weak inversion model

\( V_T \)
Process Variation

- Simulation parameters are for the “typical” process
- But what if you got the “Friday at 4:30” process?
- Foundries often provide “corner” data which attempt to represent, within device models, what are the “worst” and “best” cases. The designer needs to make sure that the design works under all of these cases (you don’t know who will be running the implanter the day of your run)

The process variation models often take the form that one flavor of transistor is “better” (or “faster”) than the other, and the cause may be correlated or anti-correlated with the other flavor. This leads to 5 cases: “typical” and the permutations of the extremes above.

- OK – so now, I understand everything, right?
Matching

◆ Not all Carthusian monks are identical – nor are all MOS transistors
◆ Directional variation of implantation across the wafer; statistics of how many dopant atoms there are...

\[ \delta V_{GS} \]

I\text{IN} \quad I\text{OUT}

Same \( V_{GS} \) ≠ Same current

PHILIPS

example 90 nm CMOS node transistor

\[ L = 40 \text{ nm (effective)} \]
\[ W = 60 \text{ nm (effective)} \]
\[ Y_{depl} = 25 \text{ nm} \]
\[ N_i = 2 \times 10^{18} /\text{cm}^3 \]

\( n_{act} \sim 1300 \text{ atoms} \)

Poisson statistics

1 \( \sigma \) fluctuation \( \sqrt{n_{act}} \sim 40 \text{ atoms} \)
Up to 33 masks in this process
Drawn Layers

Si substrate

SiO₂

Si substrate
Verification

- DRC
- LVS
Still Not Done

- Extraction (of parasitics) and “post-layout” simulation
- 2nd Order Effects are Critical in IC Design

Various other design sins not checked
Current IC Group Projects

- 4-channel CCD readout (CDS + 16 bit dynamic range digitizer) for SNAP (space qualified)
- A “high-voltage” clock driver and sequencer for the above (space qualified)
- A 16-channel higher-speed variant for almost Column-Parallel CCD readout (>100 fps / Megapixel; ≥14 bits)
- 4-channel, 10 GS/s switched capacitor array with digitizers and digital waveform accumulators
- 16x16-channel CdTe pixel readout for high-energy x-ray astronomy (space qualified)
- Monolithic detectors (see below)
Increasing Integration

1D

2D-Hybrid

Pixel Module

Pigtail (beyond)

Sensor
ASICS
Flex Hybrid (green)
Bumps
Wirebonds

Schematic Cross Section
(through here)
Active Pixels – the IC *is* the Detector

Used to replace CCDs in cheap (and now not-so-cheap) digital cameras
Also might make the ideal detectors for certain types of electron microscopy

300 keV $e^{-}$

1000 µm

$\text{SiO}_2$

$\sim 10 \mu m$

$\text{Si}$

$\sim 10 \mu m$

Heavily Doped Substrate
Well Adapted to High Sensitivity (speed)

- Thin detector
- Thin collection region within thin detector
- Gain – \( e^- \) are several times minimum ionizing: very high S/N
- Monolithic – can add on-chip electronics (ADCs, fast readout …)
- Use radiation-hardening techniques developed for HEP

300 keV \( e^- \)

40 \( \mu m \)

4 \( \mu m \) SiO\(_2\)
2 \( \mu m \) Al
2 \( \mu m \) SiO\(_2\)
8 \( \mu m \) active Si

1 \( \mu m \) active Si

Inactive Si

50 \( \mu m \) total
1st Image (200 keV)

CMOS Imager

Film

48x144
10 µm Pixels

24x72
20 µm Pixels

12x36
40 µm Pixels

Beam stop on the 200 CX at NCEM
1st Useful Detector Prototypes

- 19 µm pixels
- In-pixel CDS
- 19 µm anti-blooming pixels
- 6 µm pixels
- 10 bit ADCs on 19 µm pitch

Constructing readout and user interface software now
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore
Director, Research and Development Laboratories, Fairchild Semiconductor
Division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is in the future of electronics itself. The advantages of miniaturization will bring about a proliferation of electronics, pushing this trend into many new areas.

Integrated circuits will lead to such wonders as home computers—eight- to ten-thousand transistors connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wrist-watch may only be a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will improve channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being massed in a central unit. In addition, the internal reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various techniques which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as indispensable units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronic equipment to include increasing complexity in electronic functions in limited space with minimum weight. Several approaches were used, including microminiature techniques for individual components, thin-film structures and combination integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the key to the future is a combination of the various approaches.

The advantages of semi-insulator integrated circuits are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating this technology claim that the sensitivity of active semiconductors does not improve when attached to active semiconductors in the passive film array. Both approaches have worked well and are being used in equipment today.
Technology Node Scaling

Year


Technology Node [nm]

1000 100 10 1

International Technology Roadmap for Semiconductors

ITRS 94
ITRS 97
ITRS 99
ITRS 00
ITRS 03
CMOS Scaling

NMOS

Scaled NMOS

Channel Length $L$

Channel Length $L/\kappa$

Constant Field Scaling
Advantages of Scaling

- Speed $\sim C_{\text{GATE}} V_{\text{DD}} / I_{\text{DSAT}} \sim 1 / \kappa$
- Circuit Density $\sim 1 / A \sim \kappa^2$
- Power/circuit $\sim 1 / \kappa^2$
- Power Density (P/A) $\sim 1$

Great for digital. Just press the “zoom” button and shrink your layout!
Analog is another story.
Another Word on Matching

**Fluctuations in doping**

\[ V_T \sim \sqrt{N_a T_{OX}} \propto \sqrt{WL T_{OX}} \]

\[ \sigma(V_T) = \frac{A_{VT}}{\sqrt{WL}} \oplus S_{VT} D \]

\[ A_{VT} \propto T_{OX} \]

Scaling: \( W/L = \text{const.}, \ L \propto T_{OX} \)

But newer technologies don’t have \( A_{VT} \times L_{\text{MIN}} = \text{const.} \)

Bad for analog, worse for digital.

Digital to the rescue?

Mismatch affects this noise margin
What’s Next?

Table 59a  Single-gate Non-classical CMOS Technologies

<table>
<thead>
<tr>
<th>Device</th>
<th>Transport-enhanced FETs</th>
<th>Ultra-thin Body SOI FETs</th>
<th>Source/Drain Engineered FETs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Concept</td>
<td>Strained Si, Ge, SiGe, SiGeC or other semiconductor; on bulk or SOI</td>
<td>Fully depleted SOI with body thinner than 10 nm</td>
<td>Ultra-thin channel and localized ultra-thin BOX</td>
</tr>
</tbody>
</table>

Table 59b  Multiple-gate Non-classical CMOS Technologies

<table>
<thead>
<tr>
<th>Device</th>
<th>N-Gate (N&gt;2) FETs</th>
<th>Multiple Gate FETs</th>
<th>Double-gate FETs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Concept</td>
<td>Tied gates (number of channels &gt;2)</td>
<td>Tied gates, side-wall conduction</td>
<td>Tied gates planar conduction</td>
</tr>
</tbody>
</table>

“Scaling” and “Death of CMOS” are talks on their own…

ITRS 2003
Future for IC Design at LBL

- Keep the edge in HEP (LHC upgrades, Linear Collider)
- Astronomy – on the ground and in space
- Biology and materials – imaging detectors
  - general “smart” detectors – 2D arrays measuring (x, y, E, t)
  - specialized “smart” detectors – e.g. built-in temporal autocorrelations
  - fast detectors for dynamics – “movies”
  - high sensitivity
- R&D
  - Hybrid pixilated APDs – 2D single photon counting arrays
  - Chemfets – CMOS circuits where the conduction modulation is by (bio) chemical reaction
Electronic Technology Growth Benefits All Science at LBL

How did we get to this point?

Growth of computations/second over time

$1000 buys...

After Kurzweil, 1999
And Acknowledgements + Apologies to the IC+ES Groups

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J Stirkkinen  
C Vu  
J-P Walder  
A Whichard  
H Yaver  
S Zimmermann

Topics not suitably addressed
- CMOS scaling
- New devices
- SiGe (and other strained Si) / SOI
- Analog design problems at fine feature size
- …