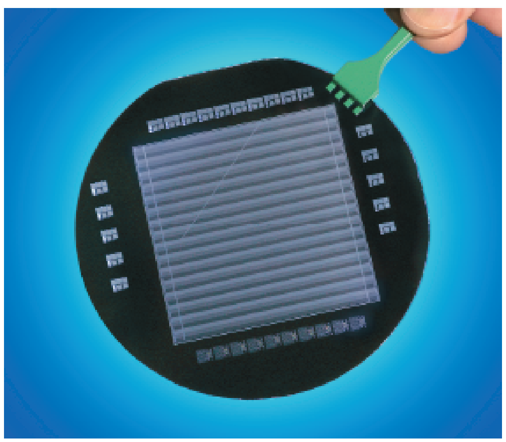
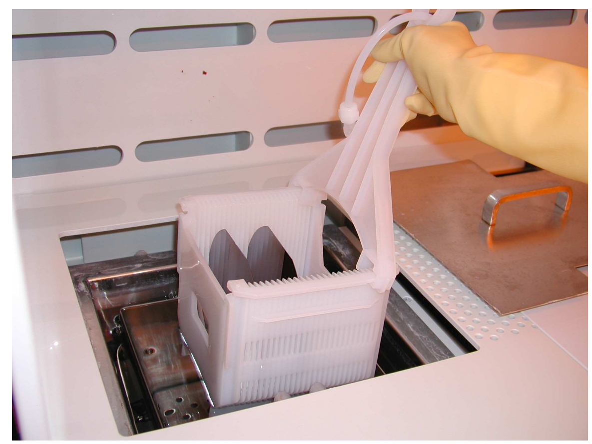
The Microsystems Laboratory – an Inside Look at Silicon Device Microfabrication at LBNL

Nick Palaio, Engineering Division 8/23/2006





What is the Microsystems Lab?

- Silicon device fabrication facility
- Specializing in detector fabrication
- Equipment and techniques to take

  wafer + CAD circuit design ⇨ finished device
- Expertise in processing ultra-pure Si
- Physics Division administration
- Operation by matrixed Engineering staff

MSL Staff

- Steve Holland – Device and process design
- Nick Palaio – Facility manager, process eng.
- Guobin Wang – Device processing and testing
- Co Tran – Device processing

- Craig Tindall – Device design and processing

Today's Talk

- MSL History
  - Notable device projects
  - Growth of the facility
- Behind the clean room walls
  - MSL infrastructure
  - Equipment and process capability
- Current and future projects/plans

MSL History

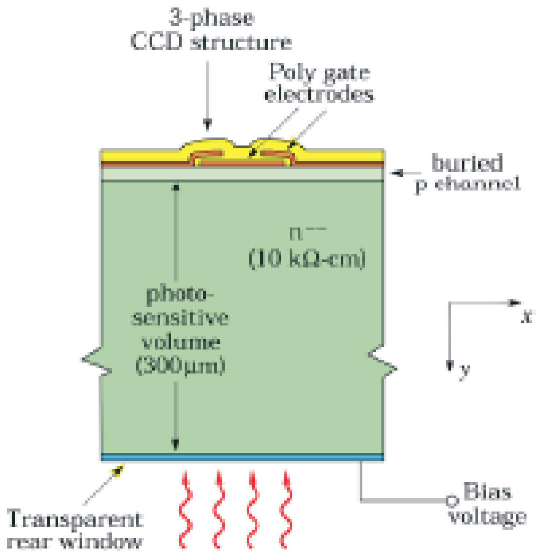
1986 → 2006

1986

- SSC – high energy physics need for silicon detectors
- Proposal for “Advanced Semiconductor Lab” at LBL
- Facility attributes
  – Dedicated to high resistivity materials
  – Ultra clean facility
  – Production styled processing

1986

Radiation detectors vs. Integrated circuits



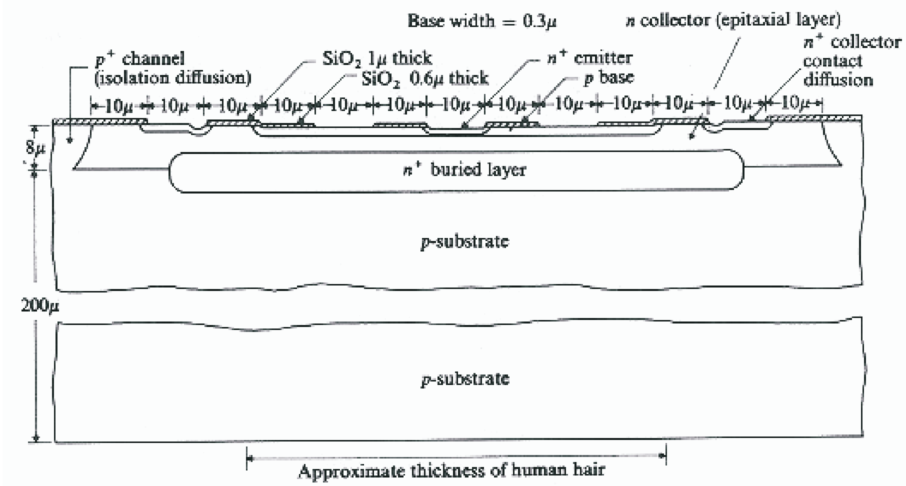


FIGURE 1-3
Cross section of an integrated-circuit transistor shown to correct scale.

Silicon radiation detector

Active through full 300um

Conventional integrated circuit

Active in only the top 10-20 um

1986

June 4, 1986

First meeting to discuss the Adv. Semi. Lab

Helmuth Spieler

Dave Nygren

Luciano Bosisio

Fred Goulding

LAWRENCE BERKELEY LABORAT
Bldg.: B90G Room: Ext.

June 4, 1986

TO: Distribution

FROM: Rich Scudero

SUBJECT: Buildings 50/70 Complex
Rehab Phase I - Semiconductor Lab

The first meeting to discuss the Advanced Semiconductor Laboratory project program and Title I design/development requirements will take place on Tuesday, June 10, at 11 a.m., in Building 70A, conference room 3377.

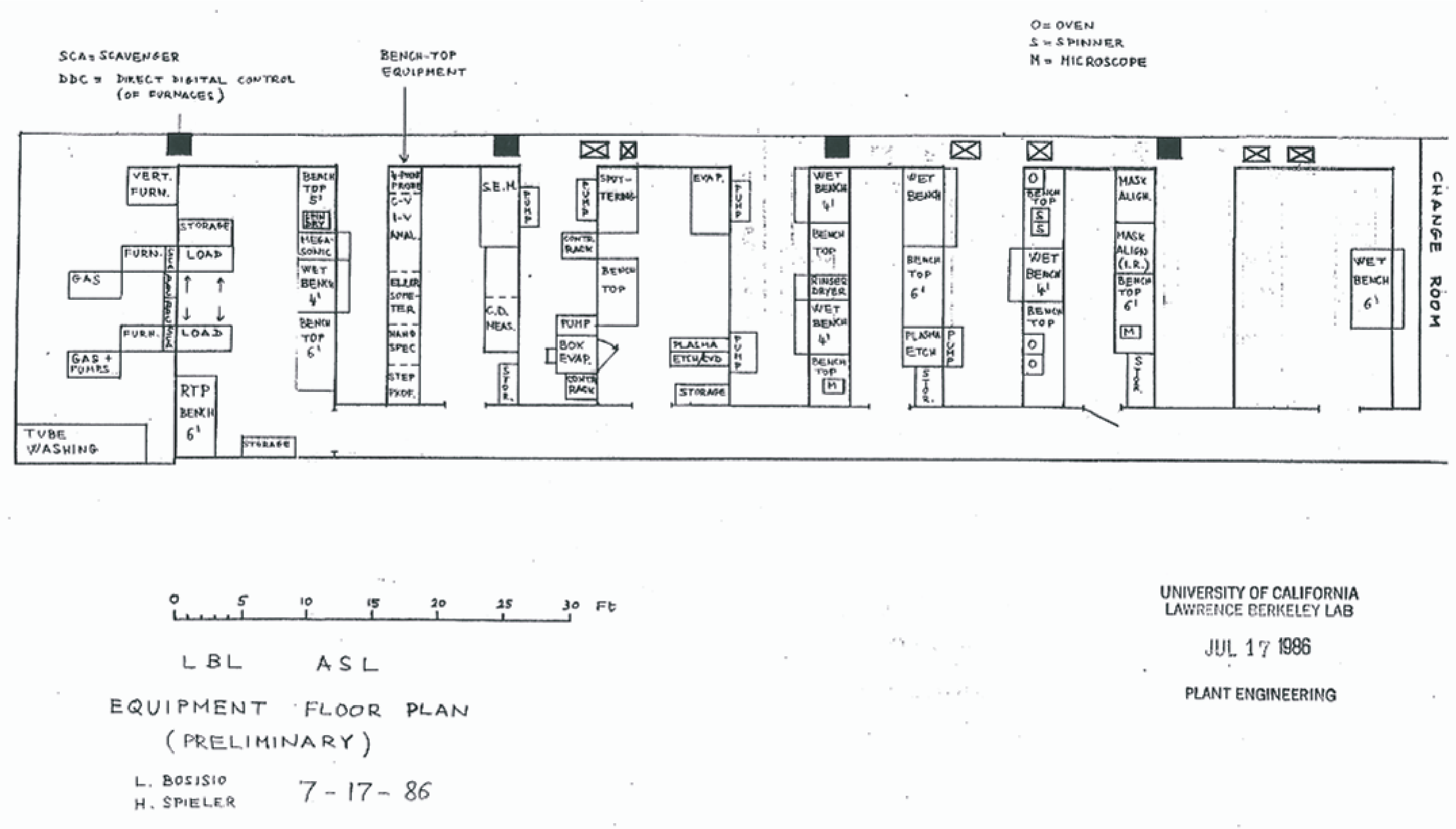
In addition to LBL scientific staff and Plant Engineering, the Architect/Engineering firm of Rasmussen, Ingle, and Anderson and LBL process consultant Jacques Beaudouin are planning to attend.

Richard D. Scudero
Plant Engineering Department

RDS:rac

c: D. Eagling
W. Ganz
R. Kropschot
D. Nygren
H. Spieler
L. Bosisio
F. Goulding

1986



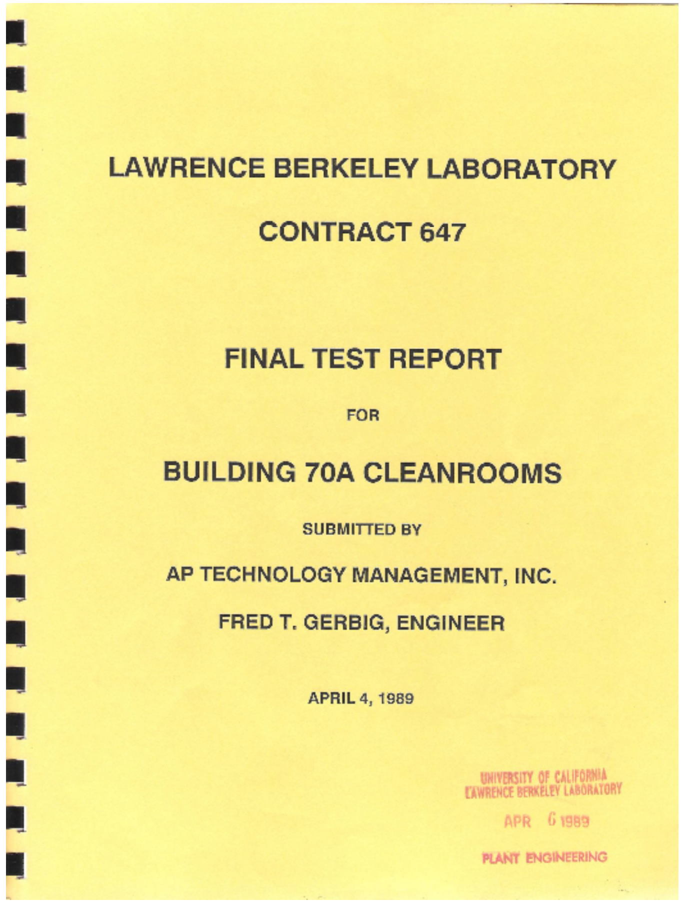
First draft MSL layout by L. Bosisio & H. Spieler

1989

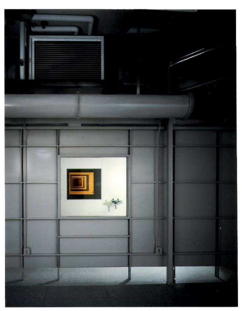
April 4, 1988

Clean room complete
and certified Class 10

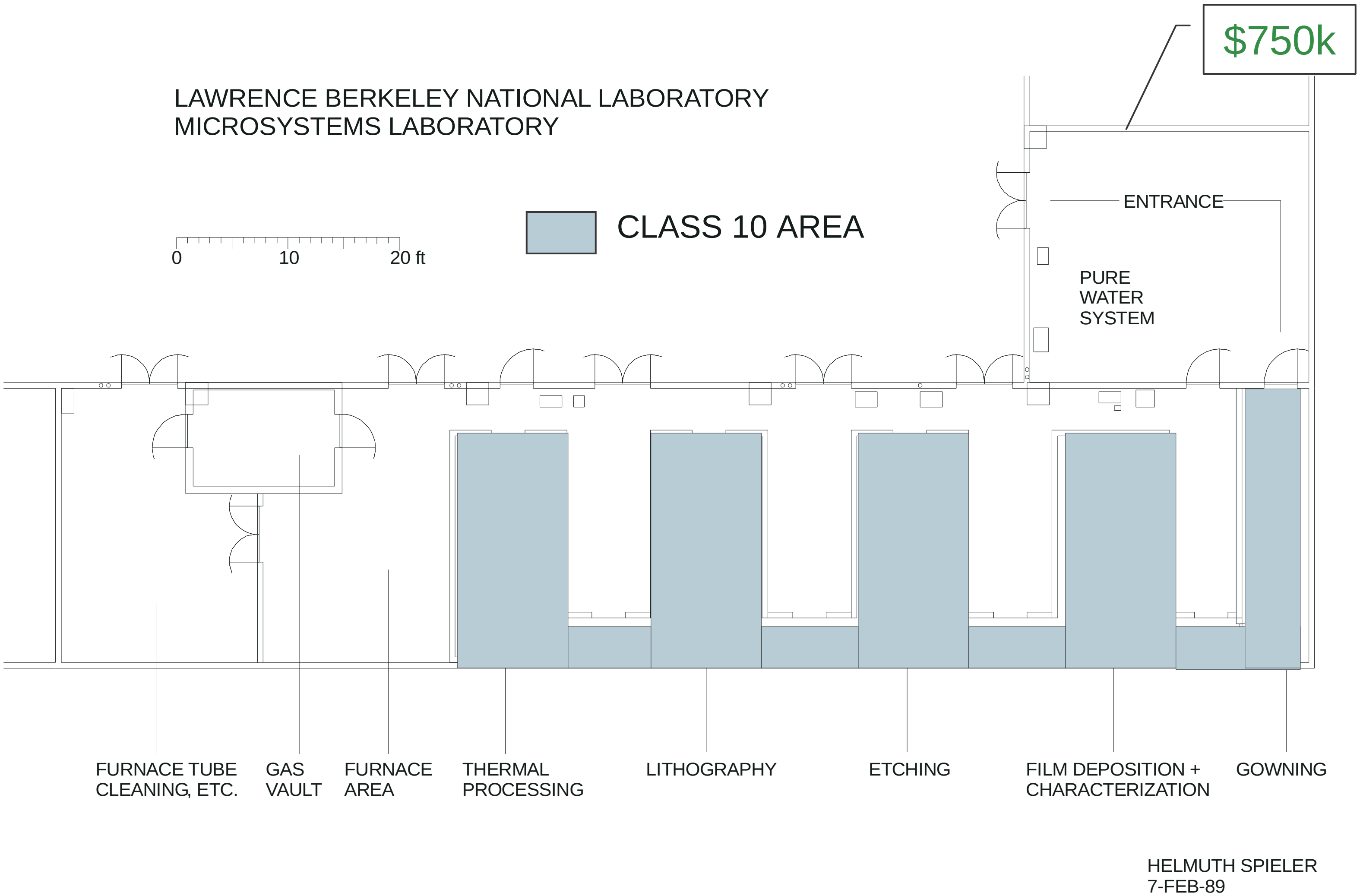
HVAC system maintains
temperature +/- 1^{o} F
humidity +/- 2% RH



1989



1989


$750k
LAWRENCE BERKELEY NATIONAL LABORATORY
MICROSYSTEMS LABORATORY
CLASS 10 AREA
0
10
20 ft
ENTRANCE
PURE
WATER
SYSTEM
FURNACE TUBE
CLEANING, ETC.
GAS
VAULT
FURNACE
AREA
THERMAL
PROCESSING
LITHOGRAPHY
ETCHING
FILM DEPOSITION +
CHARACTERIZATION
GOWNING
HELMUTH SPIELER
7-FEB-89

1990

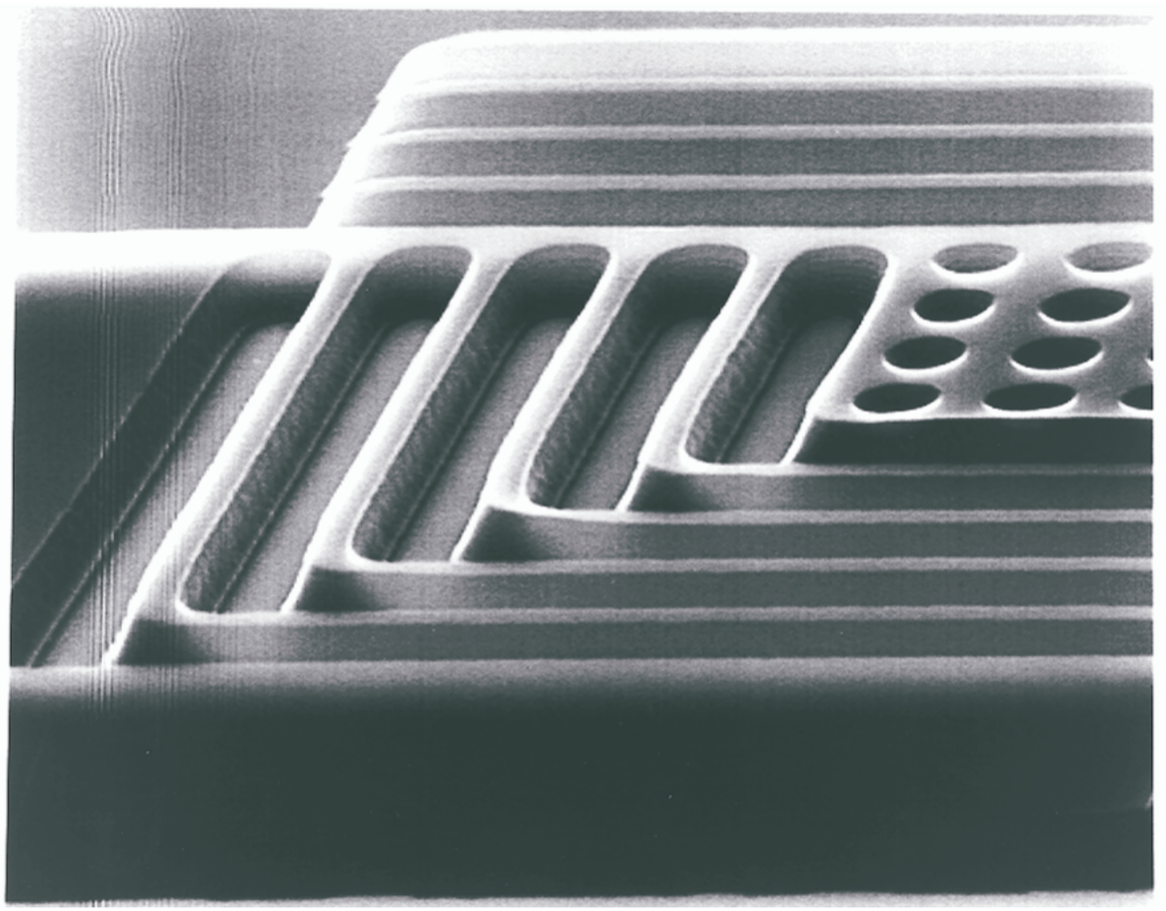
- Begin filling clean room with process equipment
- Specification, order, delivery of diffusion and LPCVD furnaces
- Donation of wafer stepper photolithography tool from Hewlett-Packard (Corvallis, OR)

1991

$0

GCA Wafer Stepper – MSL's First Production Tool

1991

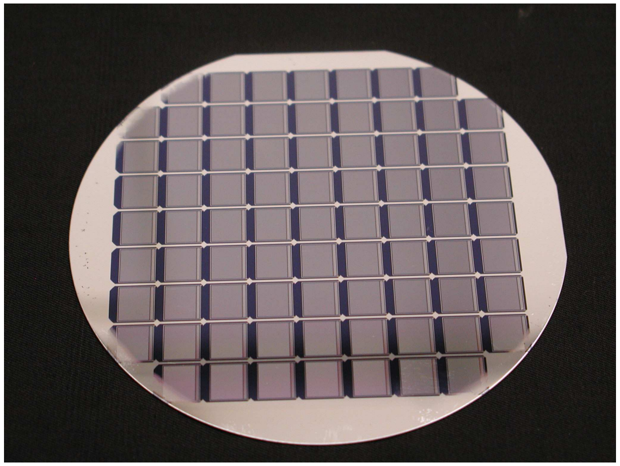


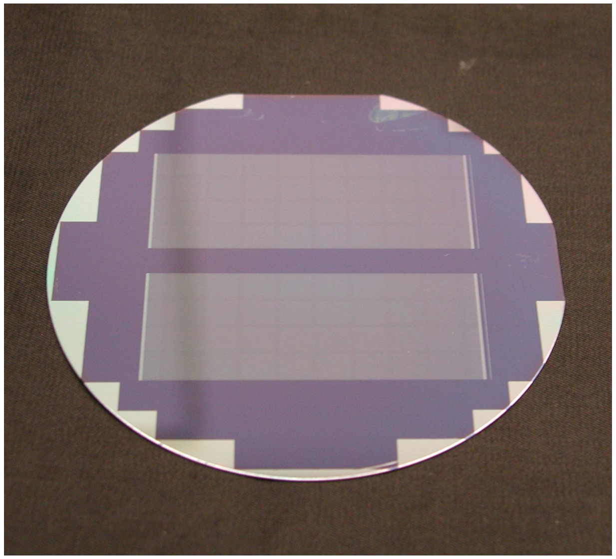
1.2 micron lines/spaces printed on the GCA wafer stepper

1991

May 1991

- MSL first device project complete
- 100mm diameter silicon wafer
- Strip detectors made using GCA stepper + campus equipment
- Large area detectors "stitched" using 2cm stepper field size





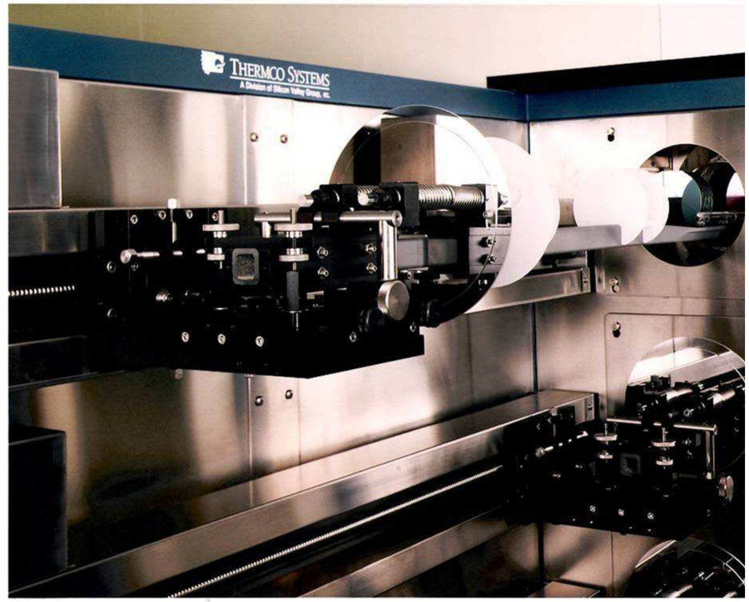
1992

April 1992

- Thermco furnaces commissioned
- Full thermal processing capability at MSL
- First polysilicon gettering run

1992

$800K

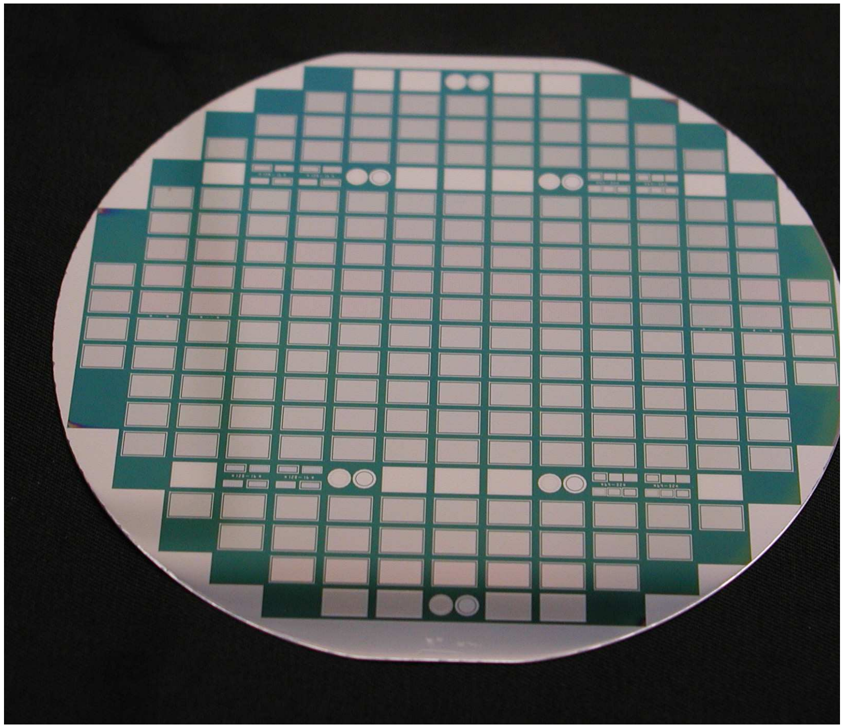


Thermco diffusion and LPCVD furnaces

1992

November 1992

- First devices made with MSL furnaces
- Pixel detectors
- 1nA/cm^2 leakage current benchmark achieved
- Metallization on campus



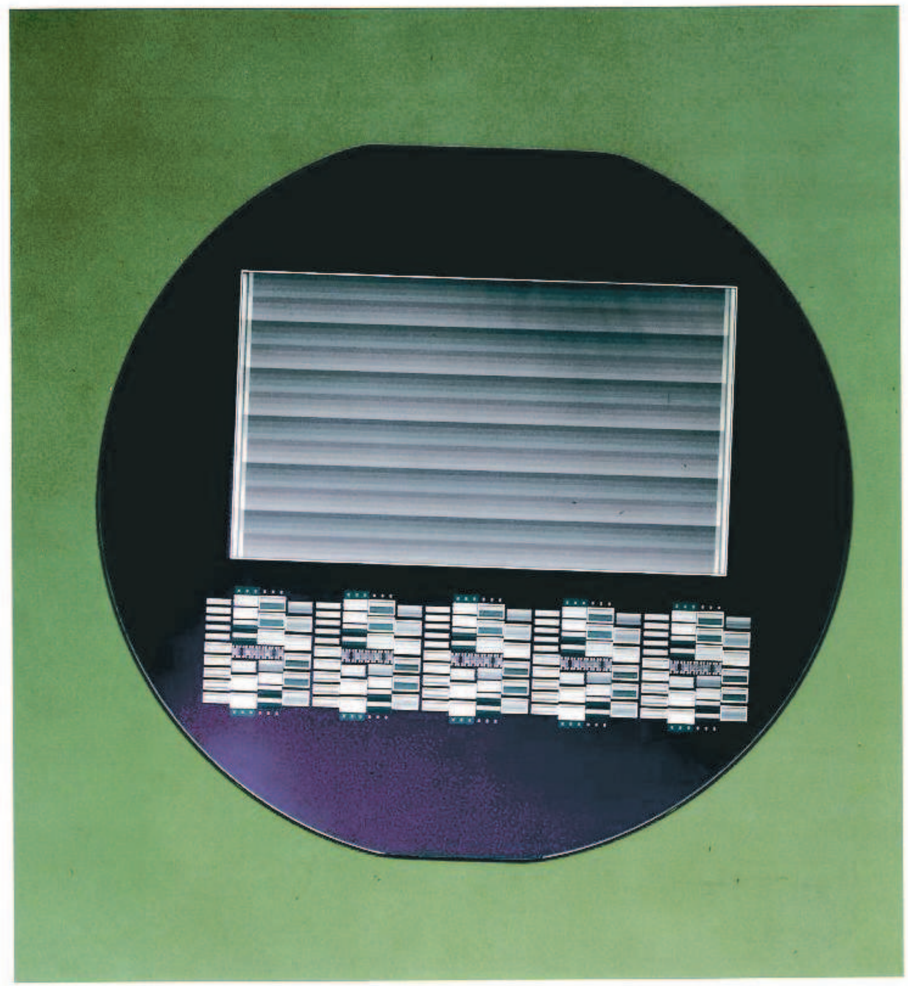
1993

April 1993

- Integrated capacitor dielectric project
- O-N-O dielectric structure fabricated
- Campus Lam Research polysilicon plasma etcher used for gate structure
- Key elements to future CCD development

1993

AC coupled strip detectors with multi-layer dielectric



1993

September 1993

- Aluminum metal deposition capability added to MSL

- MRC 603 sputtering system

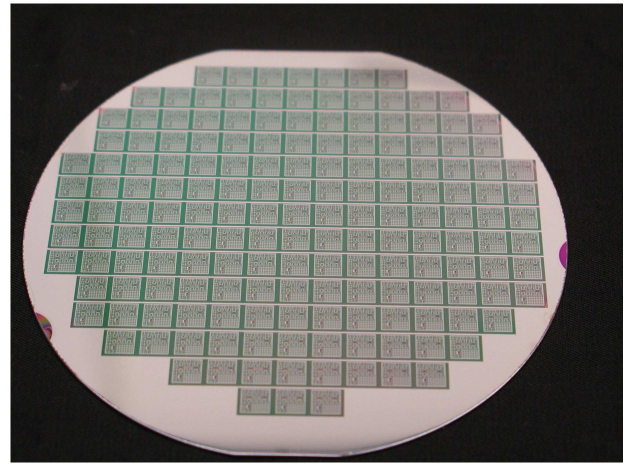
- MSL has full fabrication capability (implant contracted)

$200k

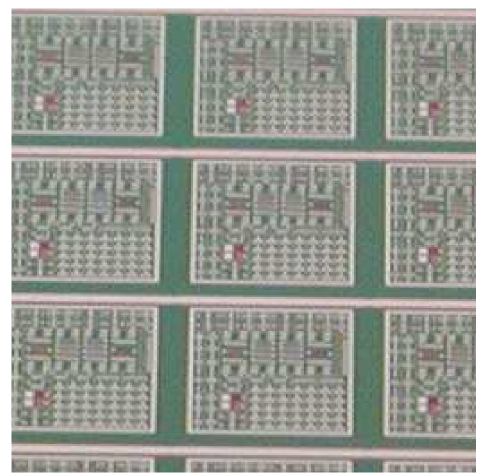
1994

June 1994

- High resistivity silicon transistors for low temperature operation fabricated



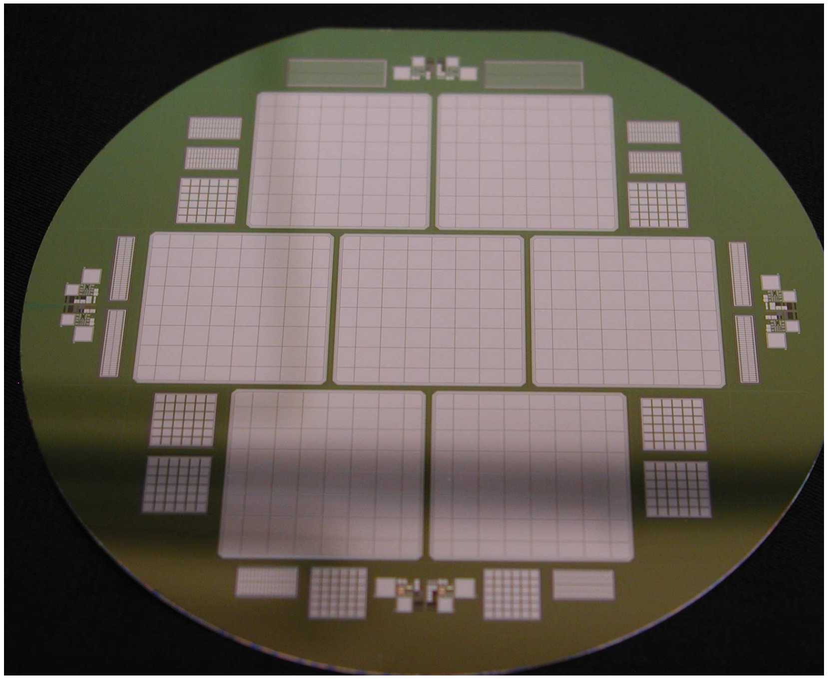
- Enable to build upon this technology for future projects



1994

August 1994

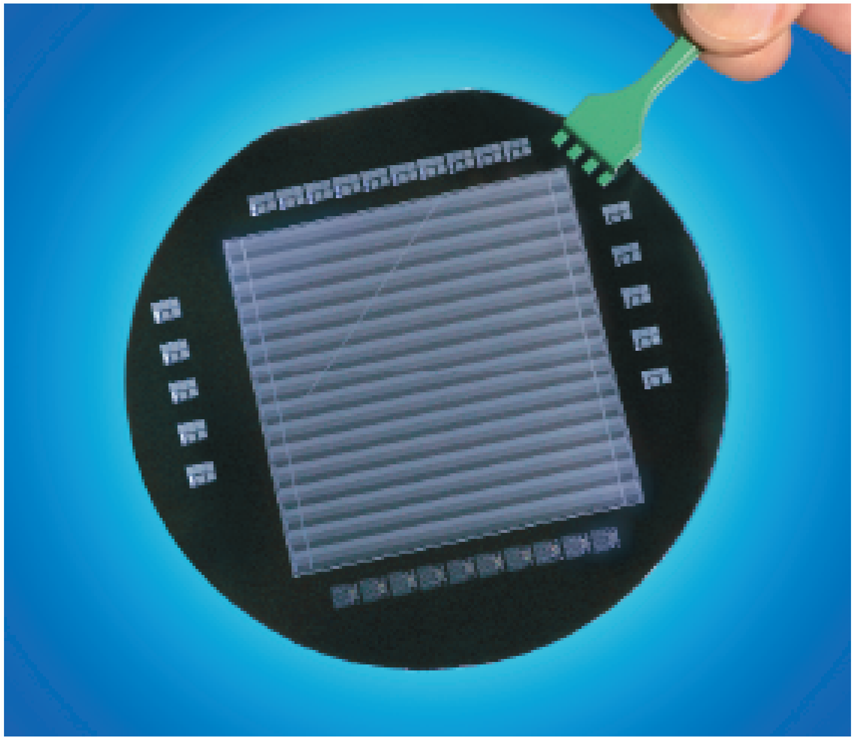
- First photodiodes fabricated
- Motivated by interest from Bill Moses, Life Sciences
- First MSL detectors for imaging



1994 - 1995

Various device projects

- Gas microstrip chambers
- P-type pixel detectors
- Strip detectors for Atlas
- X-ray detectors synchrotron applications – C. Rossington



1995

- FY1995 LDRD[1]: "Development of High-resistivity Charge-Coupled Devices for Imaging"
- Investigators: S. Perlmutter, G. Goldhaber, C. Pennypacker, H. Spieler, S. Holland, R. Stover (UCSC), industrial partner
- Also inspiration from D. Nygren
- In support of astrophysics efforts at LBL

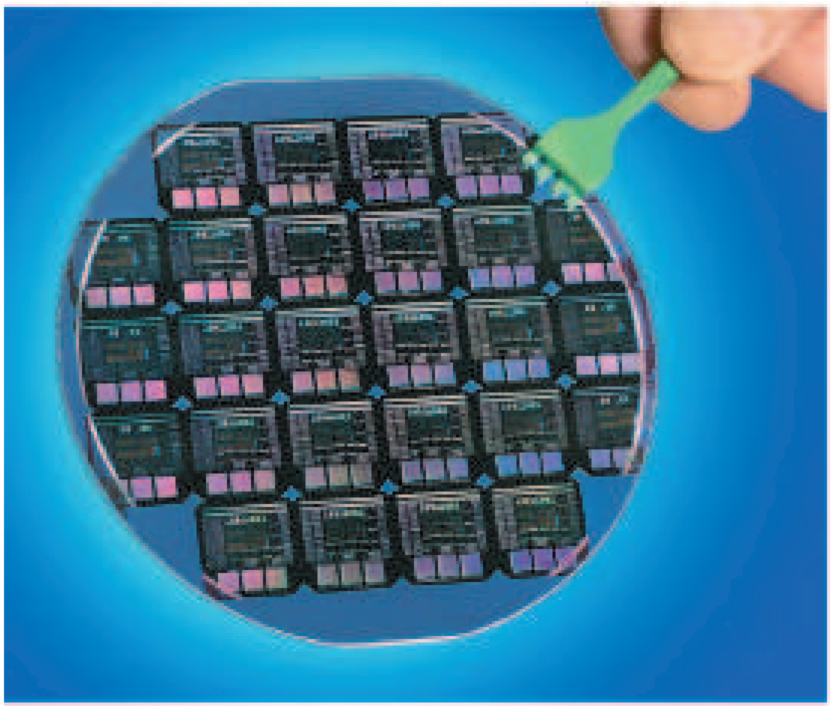
[1]Laboratory Directed Research and Development
LBNL internal funding

1996

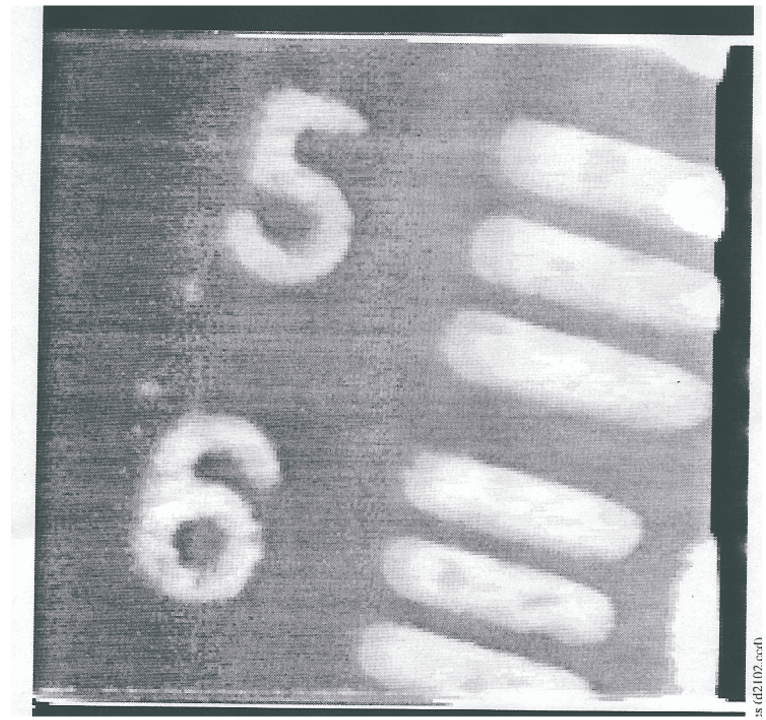
May 1996

- First charge-coupled device (CCD) fabricated in MSL
- Exploit properties of high-resistivity silicon
  - high sensitivity due to large active volume
  - reduced cost – no thinning of wafer
- Ten photomask process vs. three for strip detector
- MSL fabrication augmented by campus equipment
- It worked!

1996

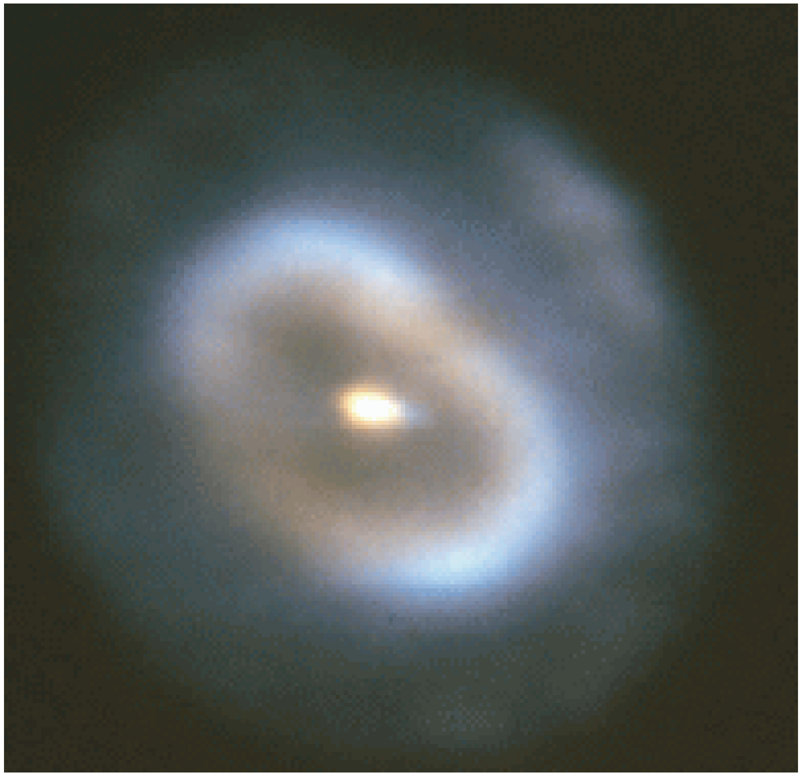


CCD wafer –200 x 200 pixel CCDs or 0.04 megapixels

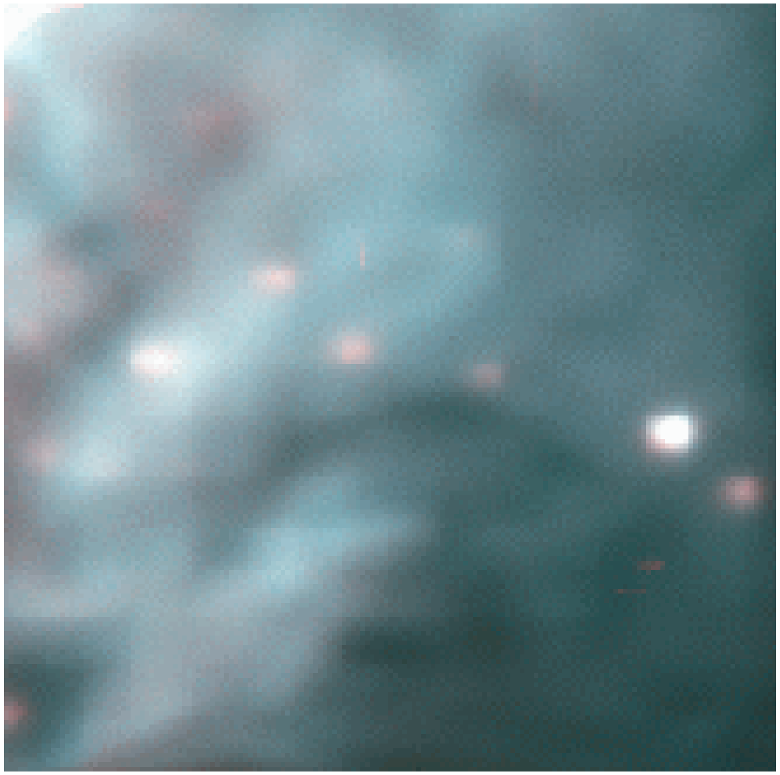


First CCD attempt images successfully on test bench at UC Santa Cruz

1996



Blue snowball nebula - Andromeda



Orion bar

Images using the first fabricated CCD from Mount Hamilton

1997

June 1997

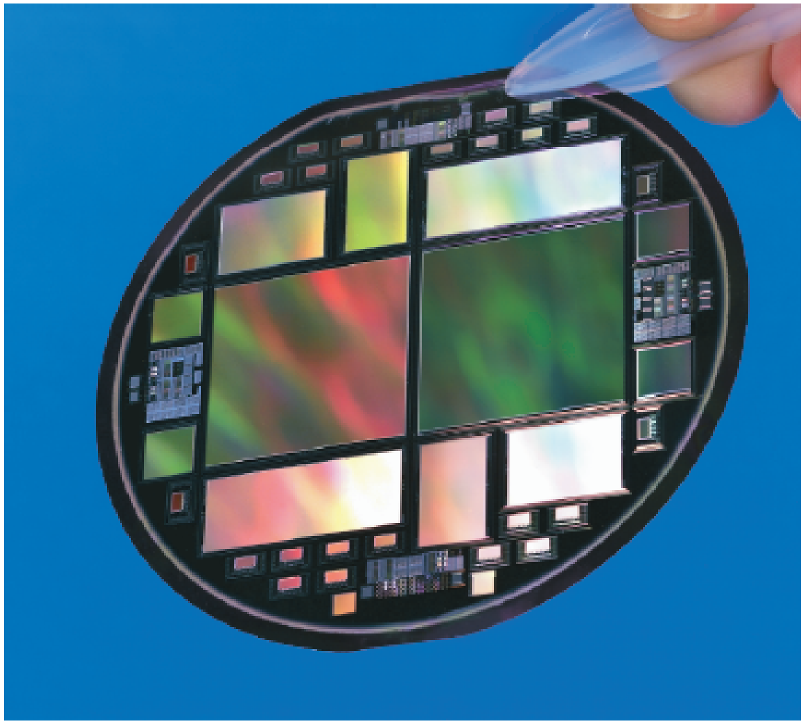
$0

- Need for large format CCDs
- MSL acquires large area mask aligner
- Intel donation via campus
- Large area detector lithography now simplified
- Replaces wafer stepper

1998

November 1998

- First large format CCD fabricated in MSL
- 2000 x 2000 pixels, 15 um
- New mask aligner used
- Critical polysilicon etching still done on campus
- Another first time success!



1998

- 2k x 2k CCD installed at NOAO, Kitt Peak, AZ
- Cover story Sept. 2001 Newsletter
- “The New Red Hot CCD”
- Image: Dumbbell nebula

1999

June 1999

• Guobin Wang joins MSL staff

September 1999

• Began fabrication of 2k x 4k CCD

Backside illumination

- Continued work on optimizing backside contact
  - Nadine Wang
- Thin polysilicon, AR coatings: ITO + SiO_2

2000

$110k

February 2000

- MSL acquires Lam polysilicon plasma etcher
- Partially funded by Keck telescope/UCO
- Critical CCD gate etching moved from campus
- CCDs now fully fabricated in the MSL

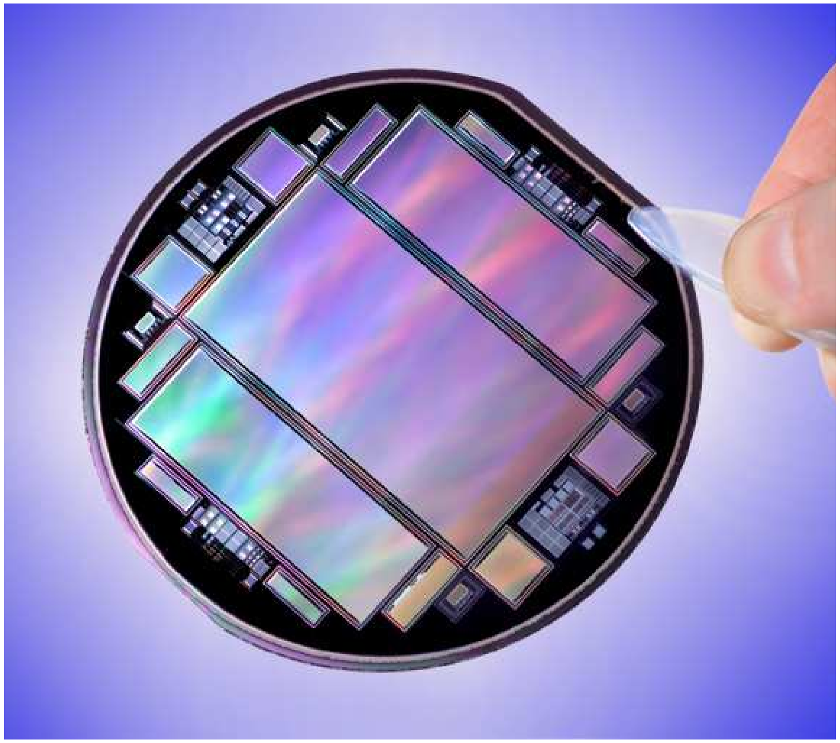
2000

<u>November 2000</u>

•First 2k x 4k CCD wafers completed

•Largest format to date

•All-MSL processed wafers



2001

- Programmatic need for larger volumes, quicker turnaround – SNAP & (later) DES
- Commercialize process
- Industrial collaboration with DALSA Semiconductor, Canada
- Shared processing DALSA-MSL
- Need to upgrade MSL to 150mm wafers

2002

June 2002

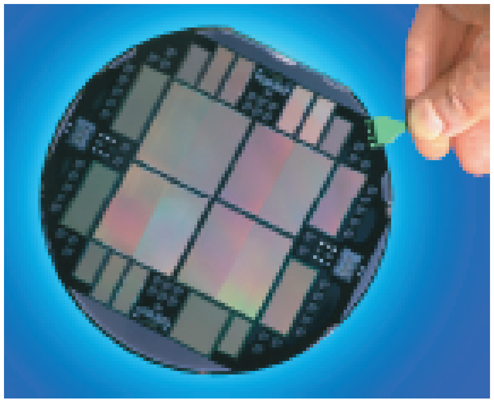
- MSL acquires 150mm compatible mask aligner

Business Model Approach

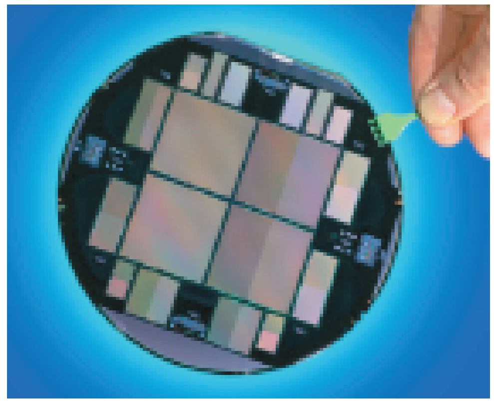
- DALSA does first 8 masking steps – std. 675um thick wafers
- Wafers thinned – 200um
- MSL finishes last 2 masking steps and completes backside contact

$365K

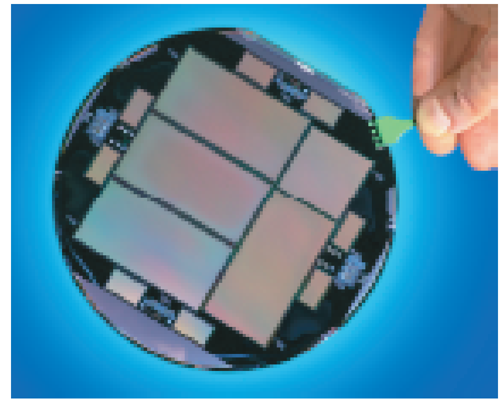
2002 - 2006



SNAP 4k x 4k



SNAP 4k x 4k



FNAL-DES 2K X 4K

DALSA-MSL “Business Model” approach

⇩

Quick design iterations – statistically significant volumes

2004

$180k

June 2004

- MSL acquires Lam 4520XLe plasma etcher
- Etching silicon dioxide contacts in CCD fabrication
- Traditional wet etching no longer viable
- Most advanced MSL fab tool

2005 - 2006

$380k

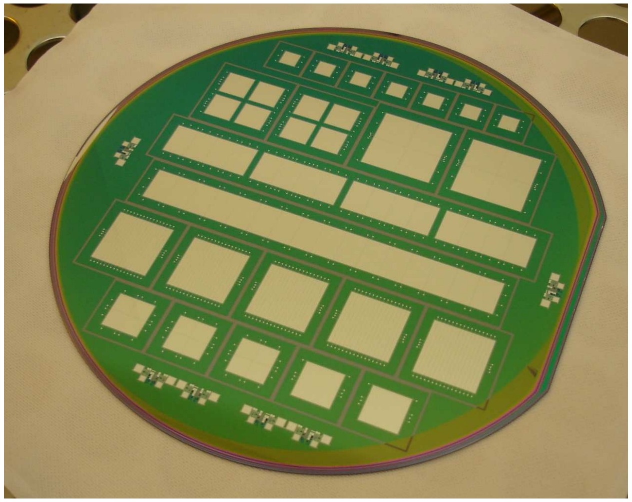
November 2005

- MSL upgrades Thermco furnaces for 150mm diameter wafers

May 2006

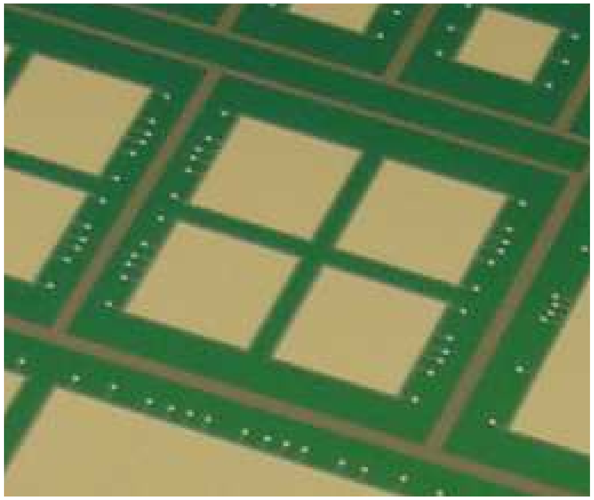
- First Business Model CCD wafers process through new furnaces
- Co Tran added to MSL staff

2006



August 2006

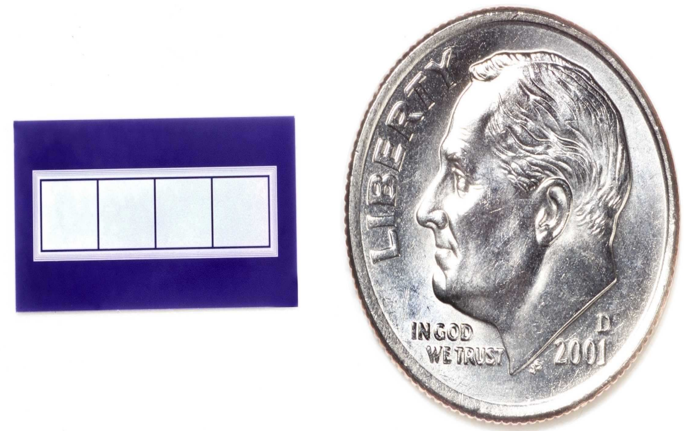
- Craig Tindall completes first MSL detector build using silicon-on-insulator technology – JPL
- Diode leakage current benchmark met



2006

September 2006

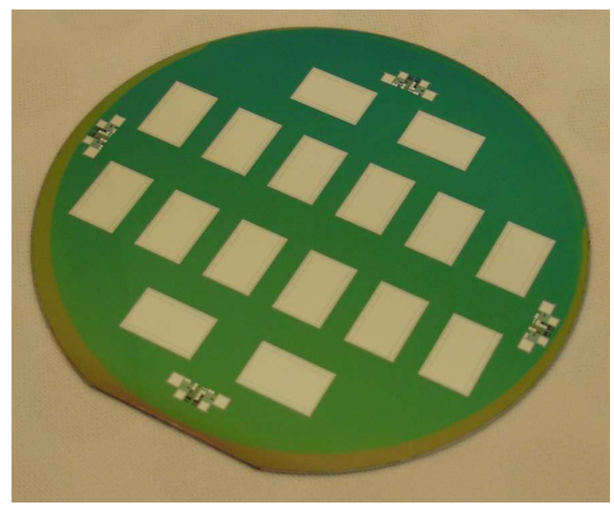
- STEREO mission launches Craig’s thin window electron detectors made in 2002
- Collaboration with SSL - first MSL devices in space



October 2006

•THEMIS mission launches with over 90 of Craig’s detectors

•SSL collaboration



Technology Transfer and Patents

June 3, 1998

- LBNL licenses photodiode process to Digirad, Corp., San Diego, CA
- Application in nuclear medical imaging
- Based on Steve Holland's U.S. Patent 6,025,585
- "Low-resistivity photon-transparent window attached to photosensitive silicon detector"

DIGIRAD
Leaders in Solid State Imaging
"Welcome to the Future of Nuclear Medicine"

Technology Transfer and Patents

June 9, 2005

- LBNL licenses CCD process to Fairchild imaging
- Based on Steve Holland's U.S. Patent 6,259,085
- "Fully Depleted Back Illuminated CCD", July 10, 2001

Microsystems Lab Facility

Behind the clean room walls

MSL Infrastructure - HVAC

- Dedicated HVAC system
- Rooftop air supply fan
- Chiller
- Humidification
- Hot and cold water piping
- Computer control system

MSL Infrastructure – DI water

$79k

- Dedicated water purification system
- 1500 gallon capacity
- Continuous flow loop throughout MSL
- No deadlegs – bacterial growth
- <100 ppt metallic contaminants

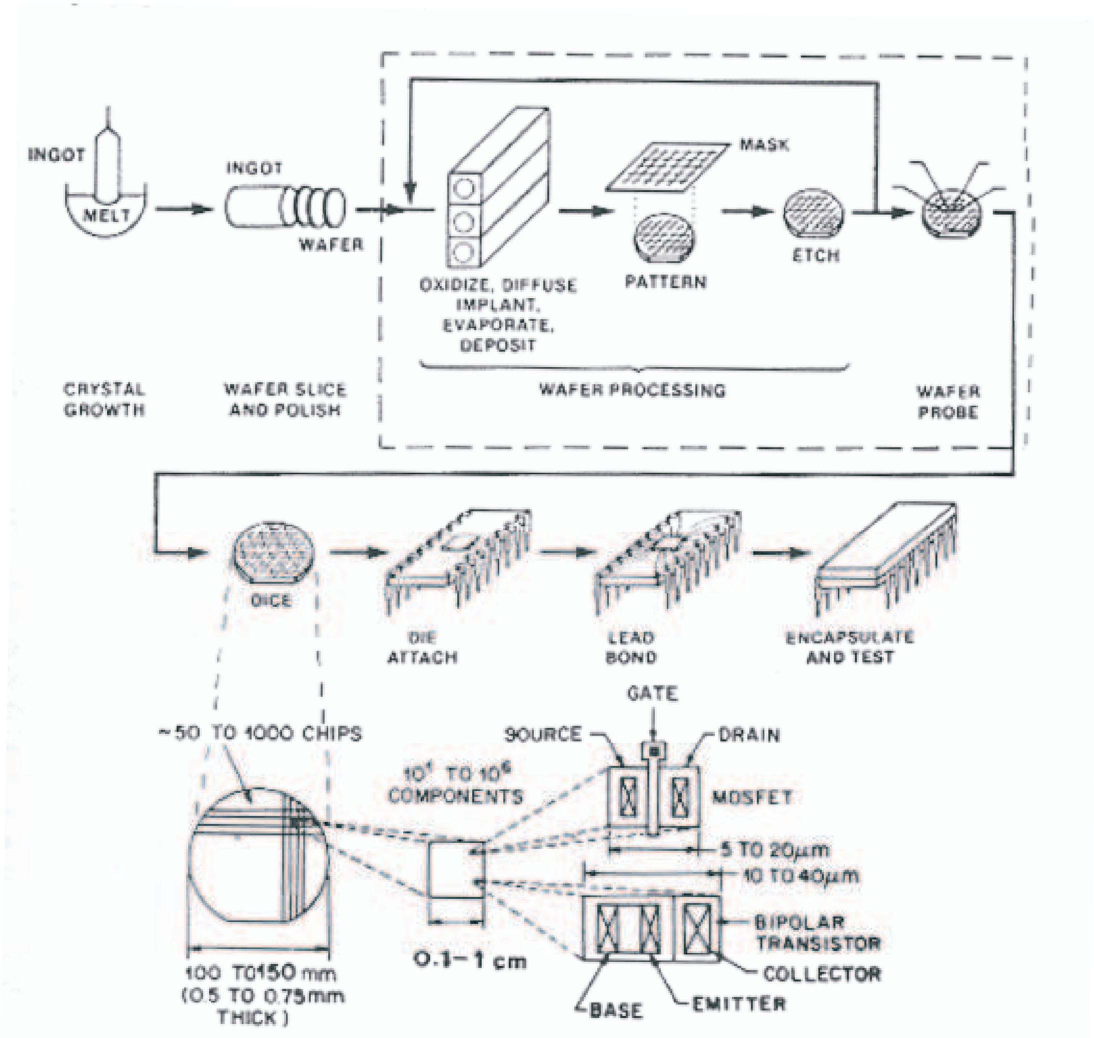
MSL Infrastructure

$50k

- Dedicated process nitrogen and oxygen lines from cryogenic tanks outside B70A

- Shared acid neutralization facility beneath B70A 1st floor parking lot

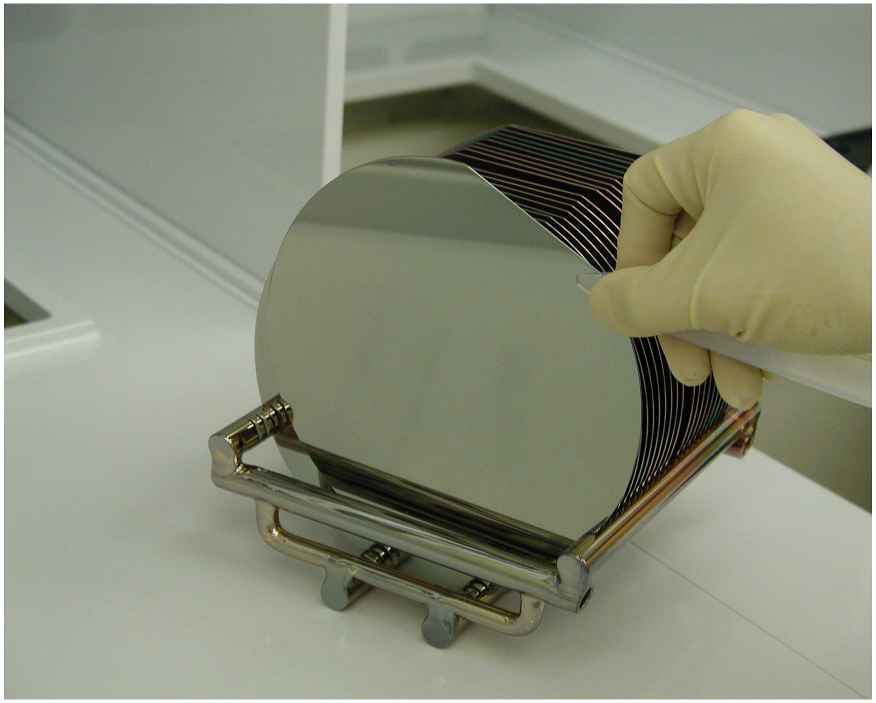
Device Fabrication Sequence



MSL – Thermal Processing

- Thermco/Expertech horizontal furnace
- Quartz process chamber – resistance heated – 425 to 1100 C
- Computer recipe-controlled processes
- Fully automated
- Wafers processed in batches – up to 50/batch – 100mm or 150mm wafers

MSL – Thermal Processing



Boat of wafers being loaded

Wafer loaded into quartz furnace boa

MSL – Thermal Processing

Furnace process capability

- Six independent process chambers
- Atmospheric processes +/-3% uniformity
- oxidation, anneal, sintering
- Low pressure process +/- 6% uniformity
- polycrystalline Si, silicon dioxide, silicon nitride

MSL – Thermal Processing

Doped polysilicon gettering process

- 1 micron film on the back of wafer
- Traps electrically-active impurity defects during thermal processing
- Maintains impurity levels at 0.1 ppt in the bulk silicon
- Low p-i-n diode leakage current – $1nA/cm^2$

MSL – Gas Handling

- Furnaces require variety of hazardous gases
- Silane – explosive, phosphine – highly toxic
- Double contained gas lines
- 24/7 facility and gas detection
- Automated gas shutoff

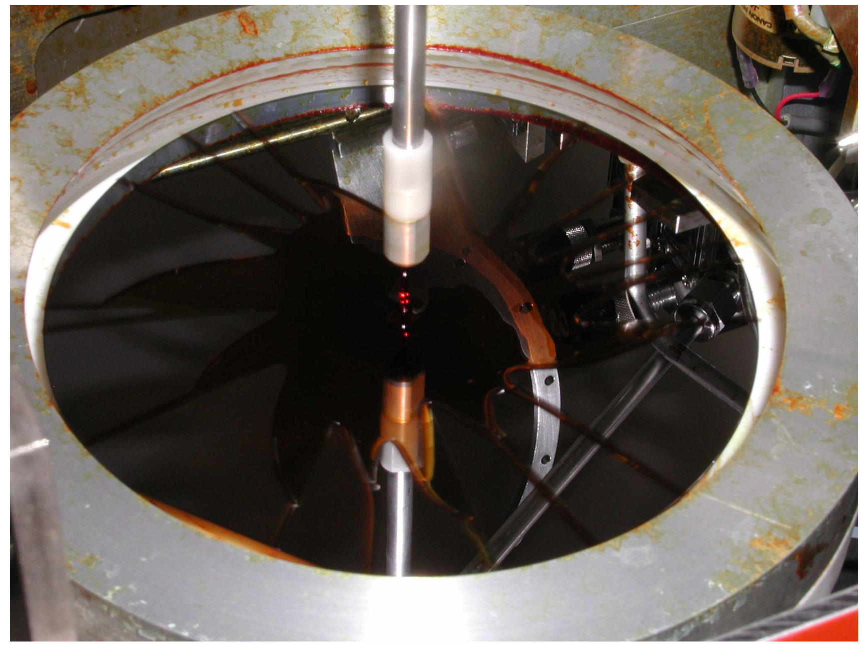
$80k

$50k

MSL – Photolithography

Process sequence

$60k

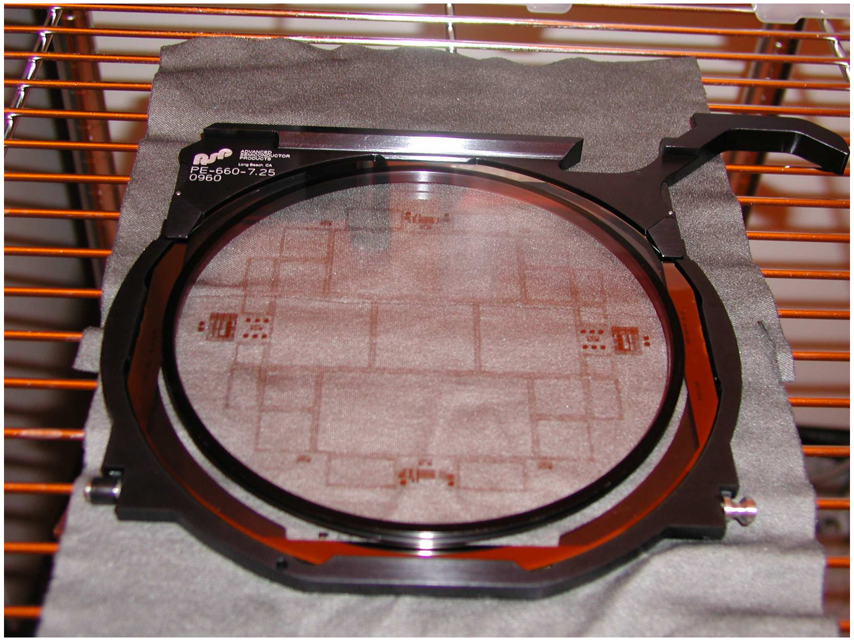


$18k

Vapor prime → Photoresist coat →

MSL – Photolithography

Process sequence



$2900/mask

Align wafer to mask and expose

MSL – Photolithography

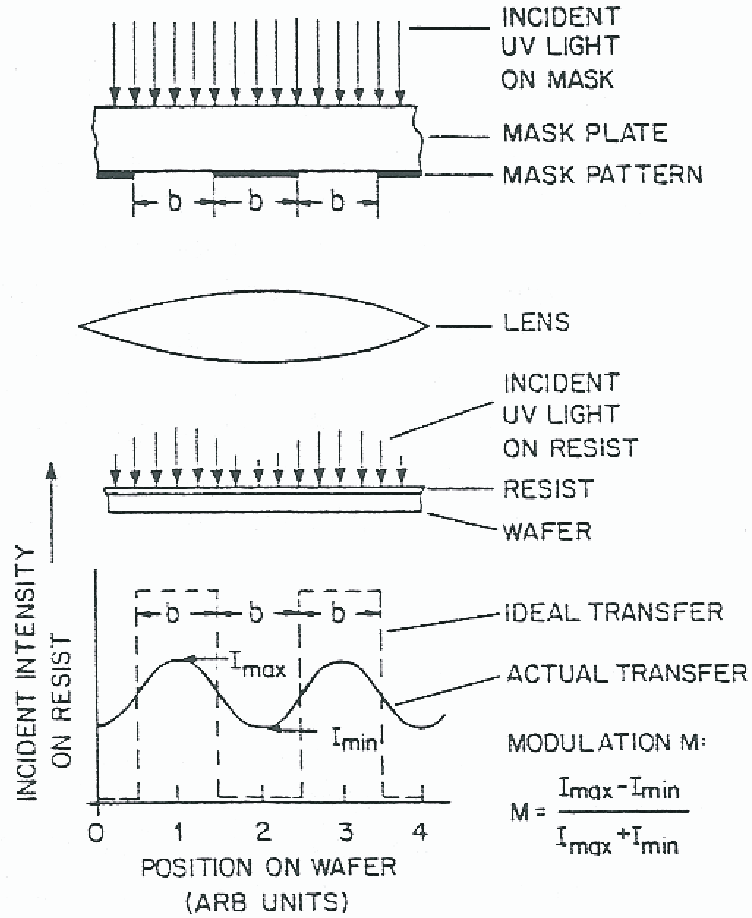
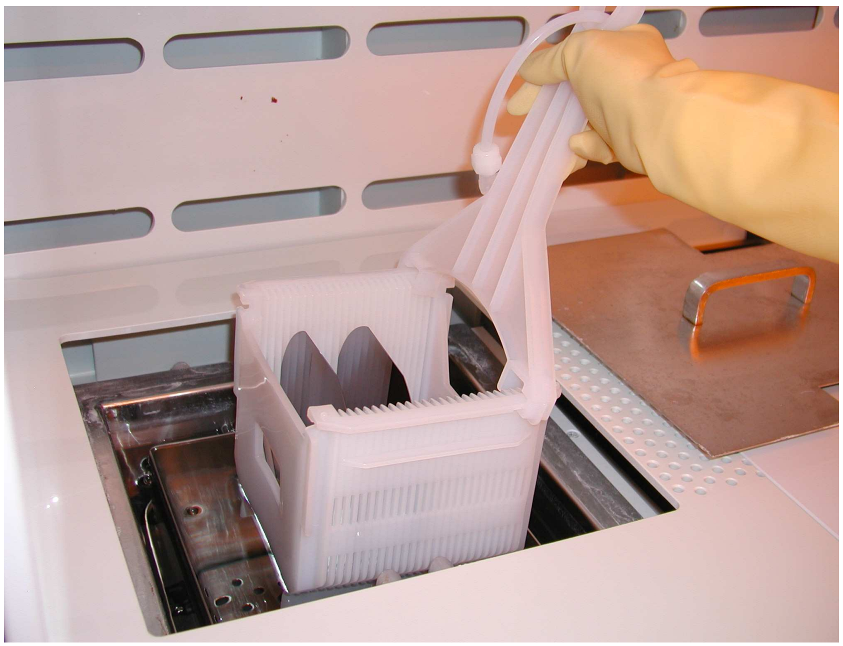
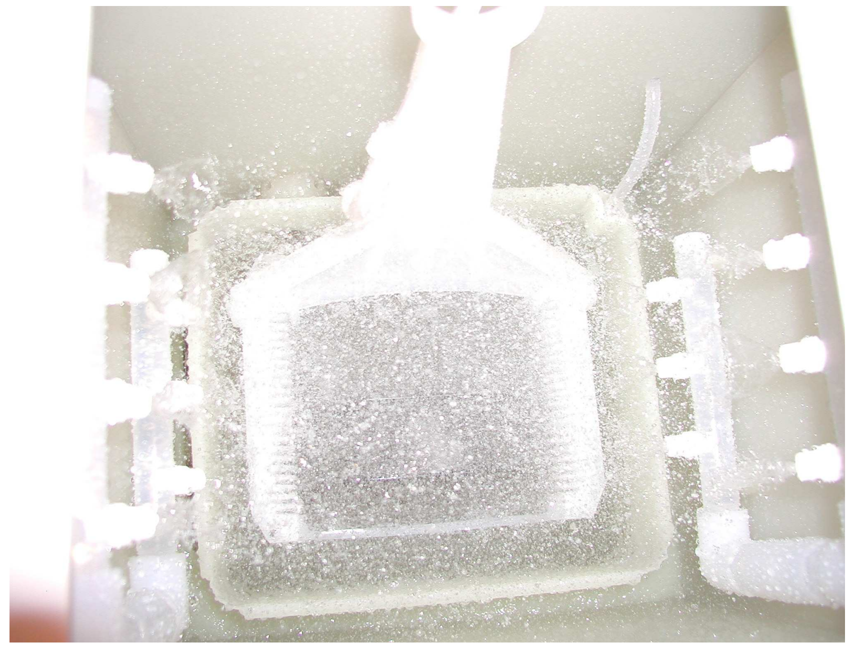


Fig. 8 Schematic representation of image transfer efficiency for a 1:1 projection printer. Reprinted with permission of the publisher, the Electrochemical Society.

MSL – Photolithography

Process sequence





Develop photoresist ⇨ Rinse wafers ⇨

MSL – Photolithography

Process sequence

$14k

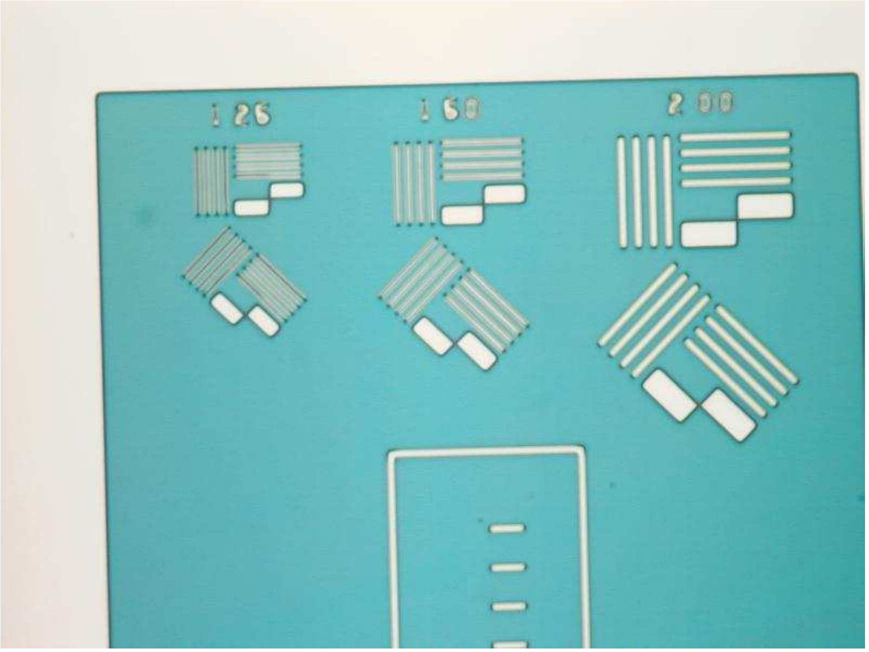
Dry wafers →

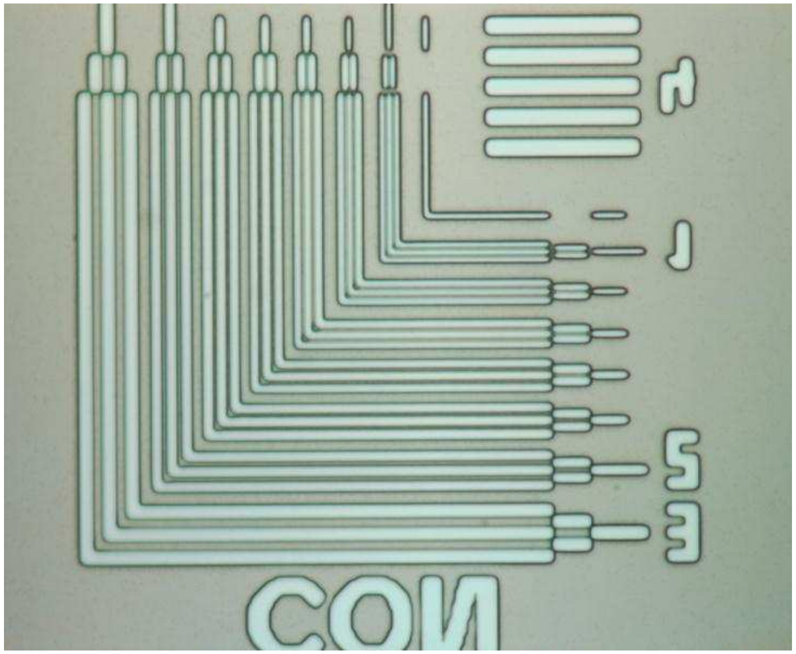
$20k

Microscope inspect

MSL – Photolithography

Wafer inspection

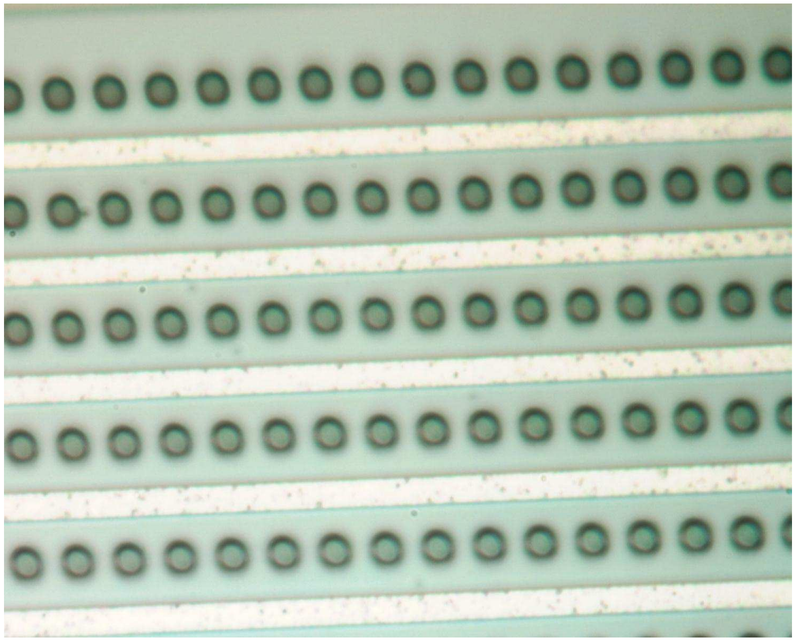




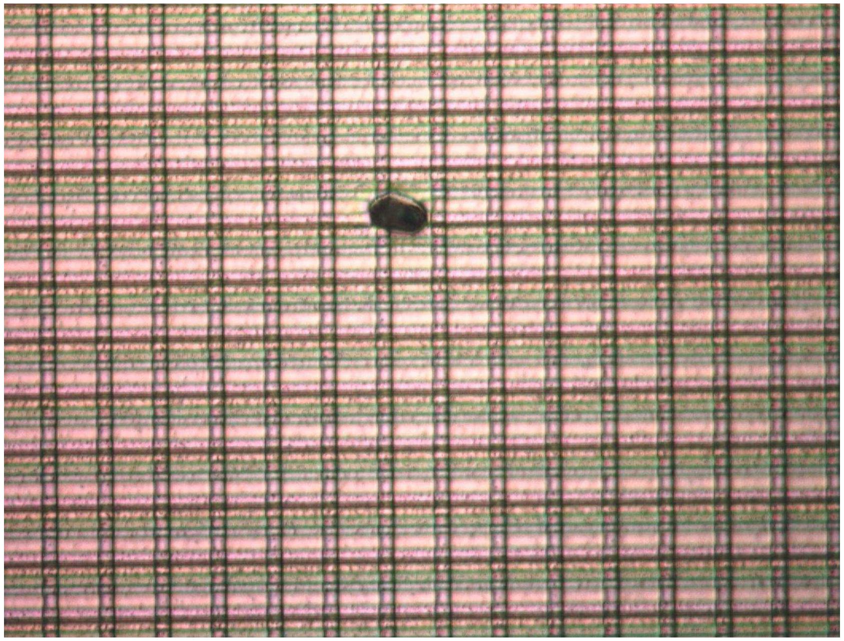
Resolution patterns – 1.25 micron lines/spaces

MSL – Photolithography

Wafer inspection



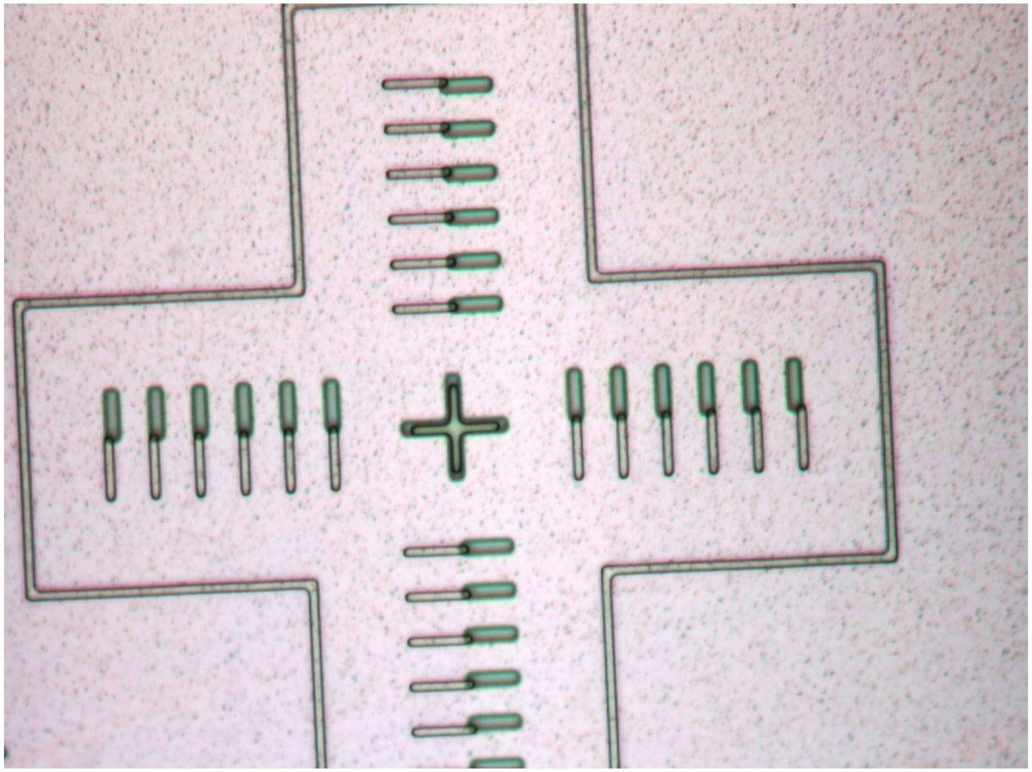
2um contact in resist



Seldom-seen defect

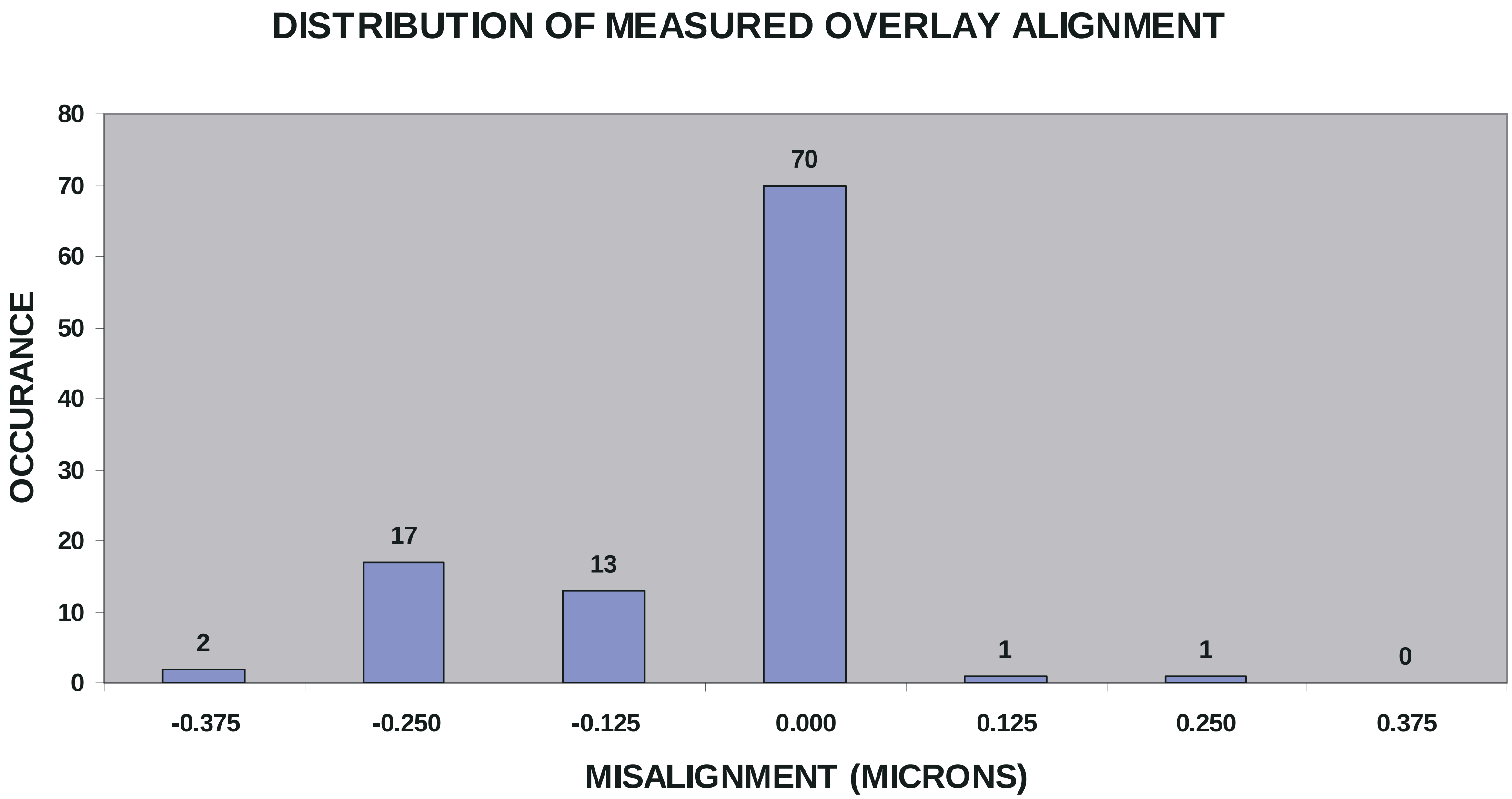
MSL – Photolithography

Wafer inspection



Resist pattern aligned to existing pattern on wafer

MSL – Photolithography



MSL – Wet processing

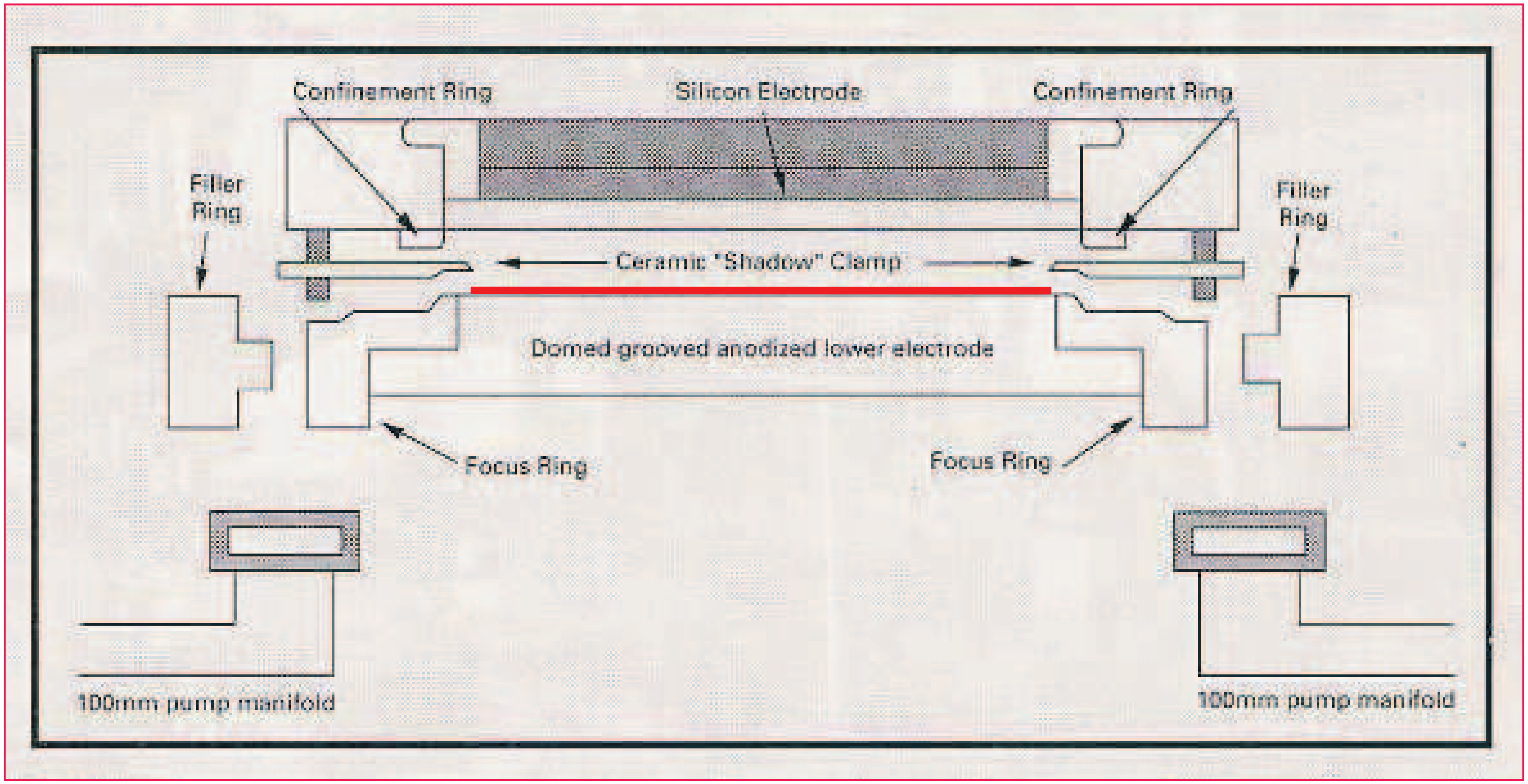
- Santa Clara Plastics wet benches
- Dedicated baths – filtered, temperature-controlled
- Pre-furnace clean – RCA I/II w/megasonic
- Etching – SiO_2, Si_3N_4, Al, Si, photo strip

$250k

MSL – Dry etching

- Superior dimensional control vs. wet etching
- High selectivity to underlying material
- Use a rf generated plasma of reactive gas to etch exposed surface of the wafer
- Photoresist protects other areas
- Two plasma etchers – polysilicon and silicon dioxide

MSL – Dry etching

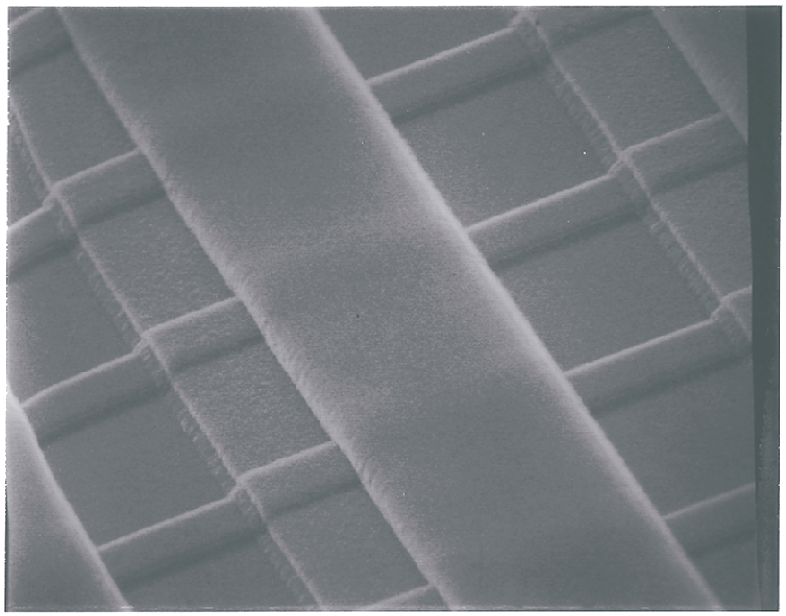


Schematic cross-section of plasma etching chamber

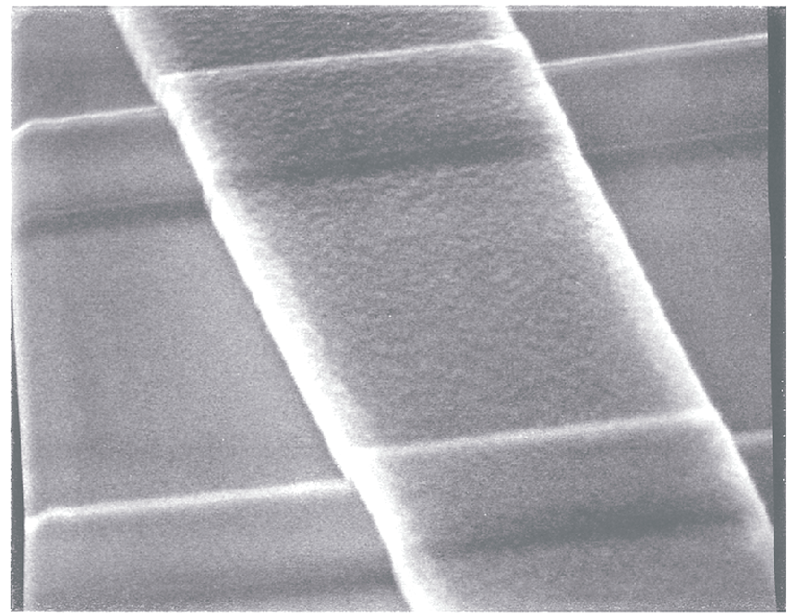
MSL – Dry etching polysilicon

- *<u>Lam 4400 polysilicon etcher</u>*
- Chlorine and Hydrogen bromide chemistry – highly selective
- Used three times in CCD process to pattern overlapping gate structures

MSL – Dry etching polysilicon

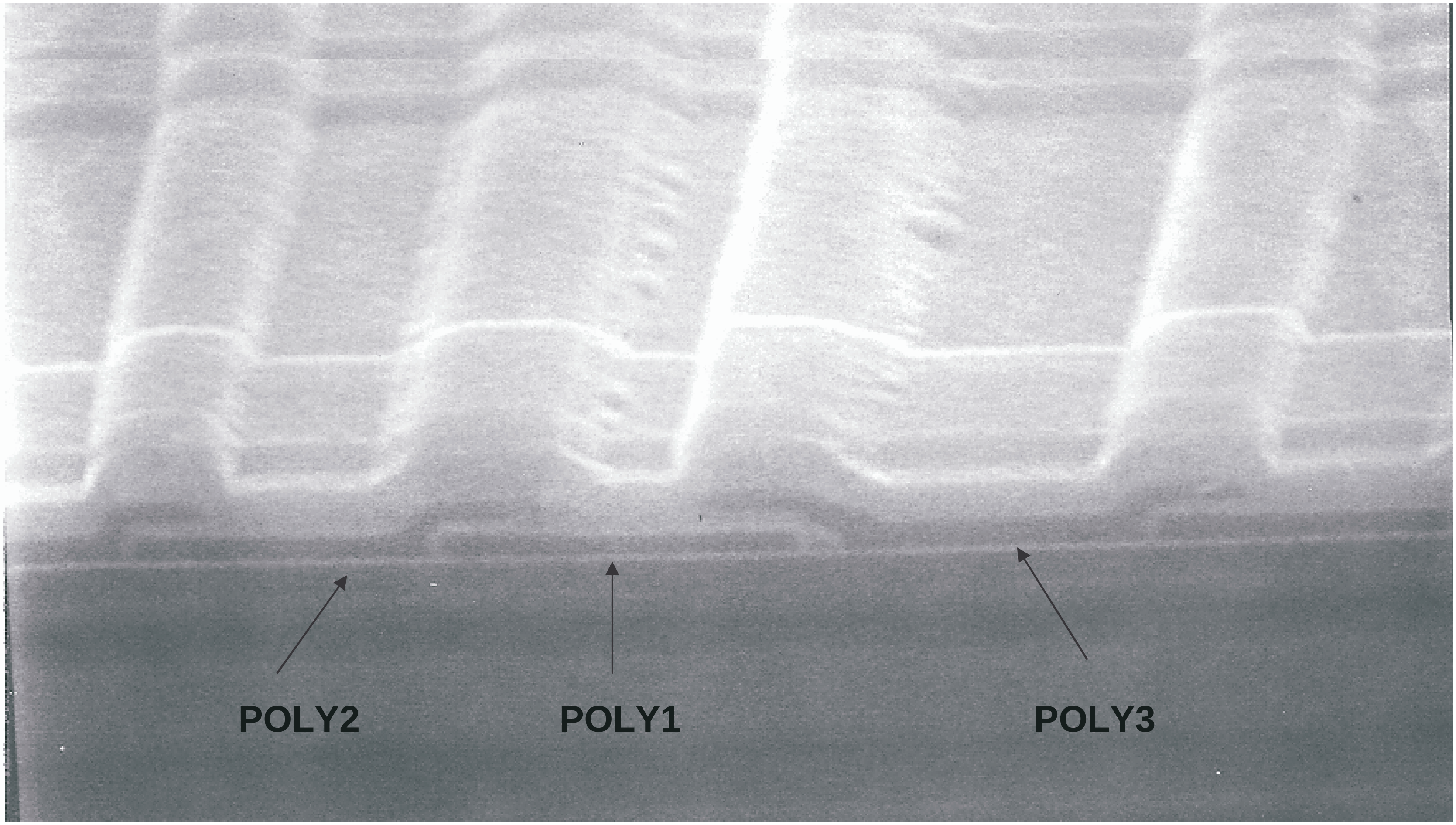


Two overlapping polysilicon gates



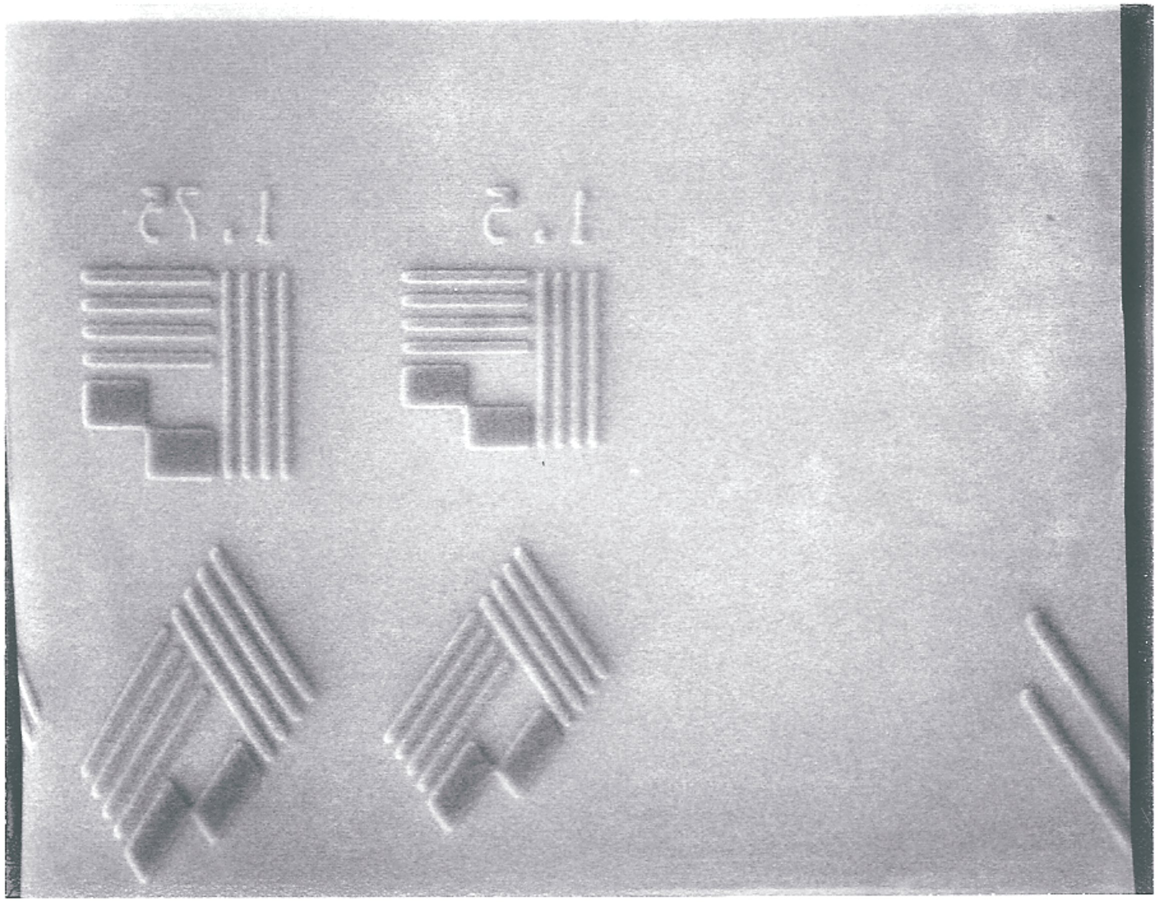
Single 5um polysilicon gate

MSL – Dry etching polysilicon



Three overlapping poly gates - CCD

MSL – Dry etching polysilicon

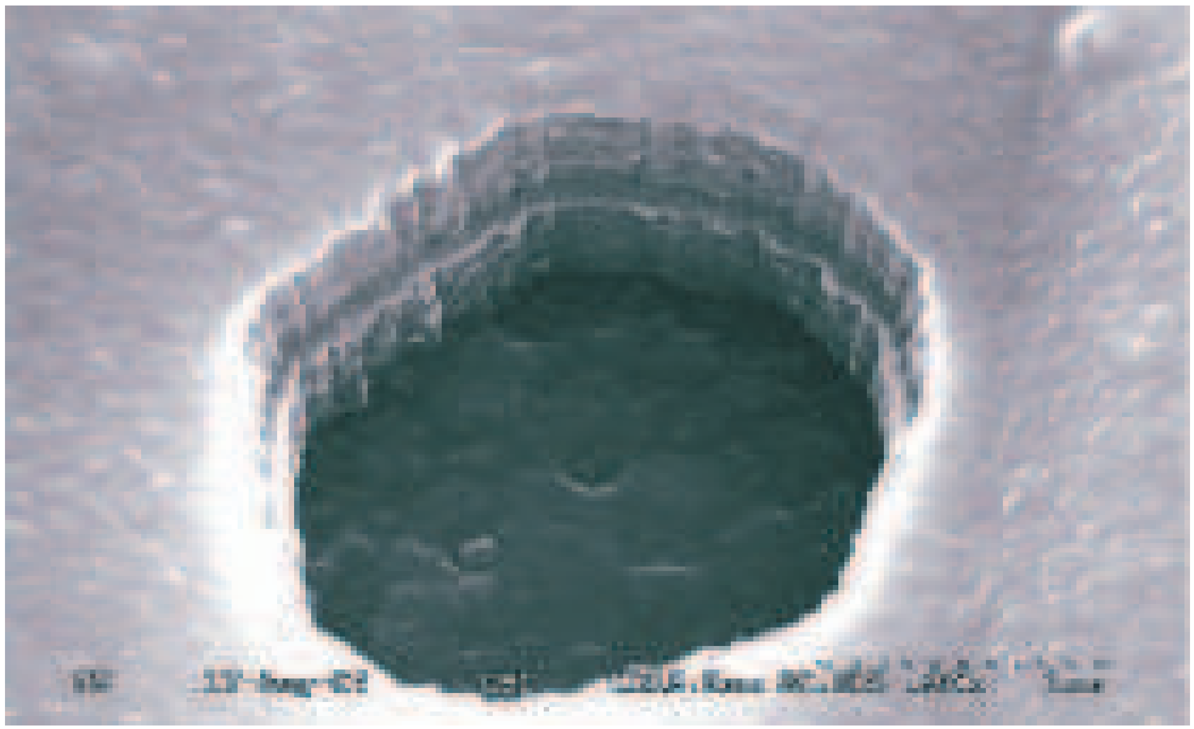


1.5 um poly lines and spaces

MSL – Dry etching SiO_2

- ***Lam 4520XLe silicon dioxide etcher***
- Freon chemistry
- Tight dimensional control maintained
- One micron thick CCD contact etch
- Dual frequency plasma for low damage

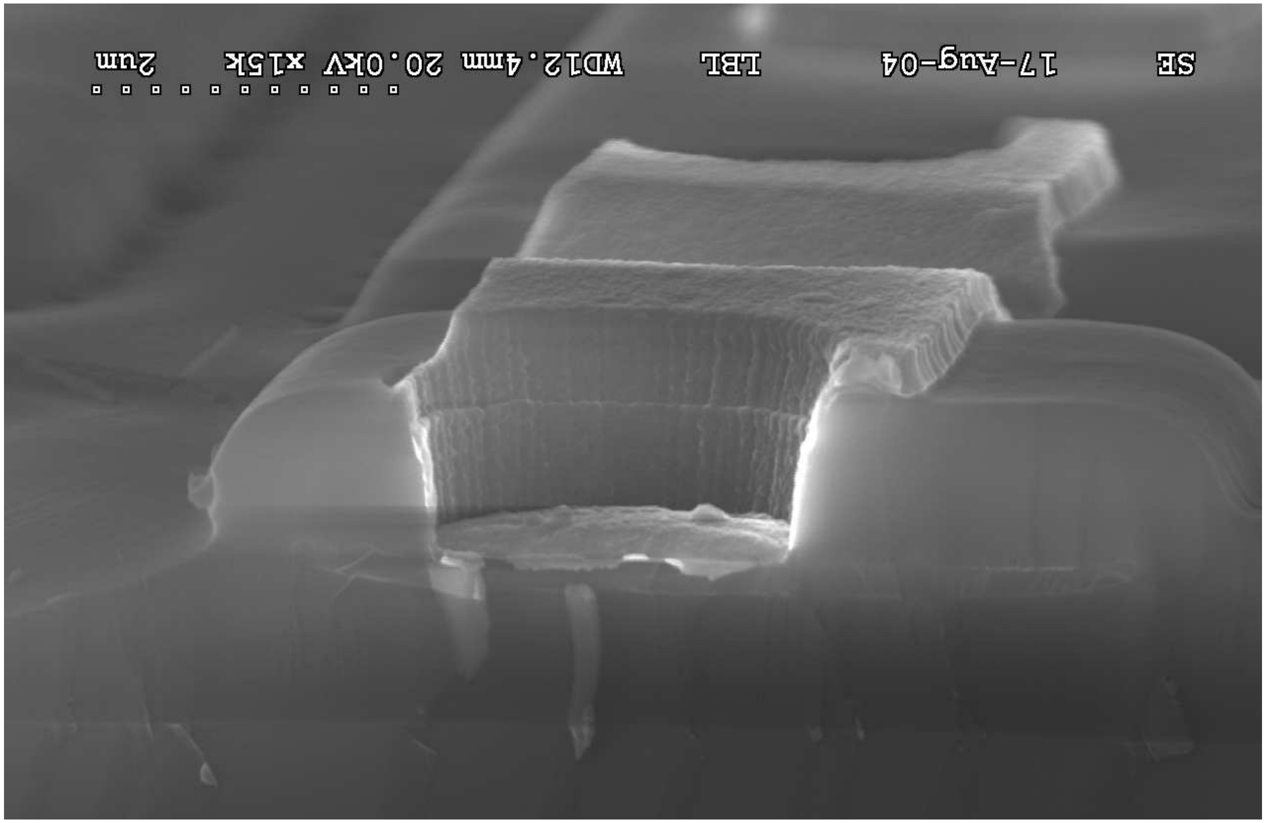
MSL – Dry etching SiO_2



SEM by Eduardo Saiz

Two micron contact etched in SiO_2 after Al deposition

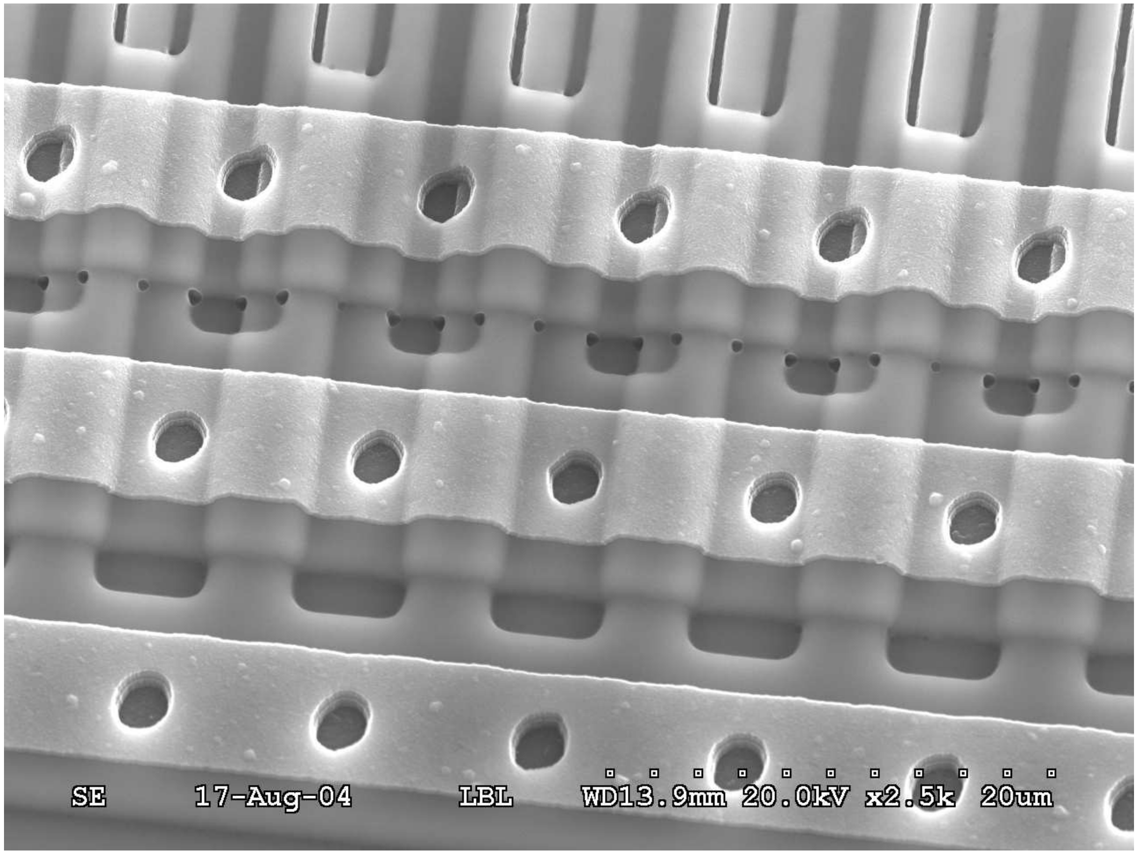
MSL – Dry etching SiO_2



SEM by Eduardo Saiz

Two micron contact in full cross-section

MSL – Dry etching SiO_2

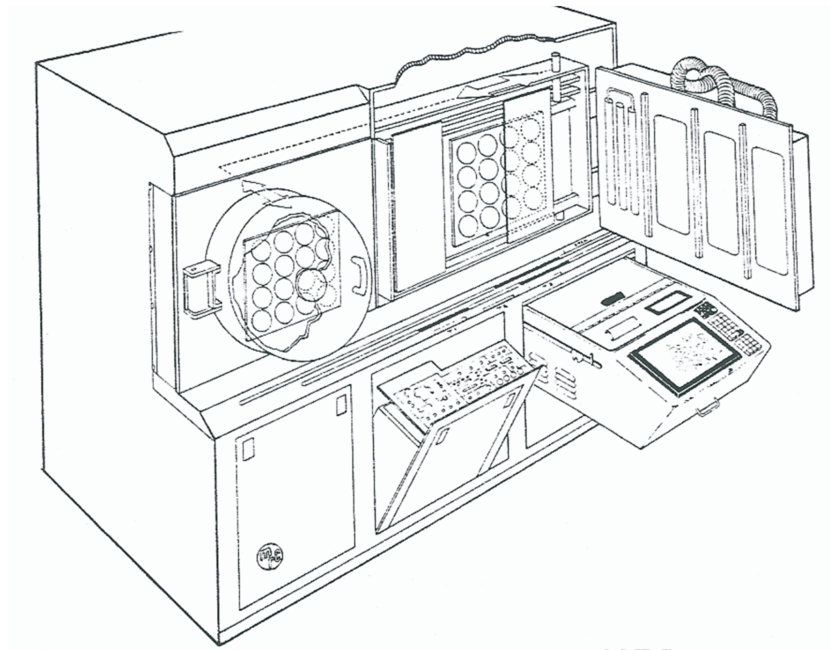


SEM by Eduardo Saiz

Making contact to 3 poly gates of the CCD

MSL – Sputter deposition

- ***MRC 603 Sputter deposition system***
- Vacuum rf plasma system
- Argon ion accelerated toward target material
- Material ejected and migrates to wafer
- Aluminum metallization
- ITO and SiO_2 optical coatings



MSL – Sputter deposition

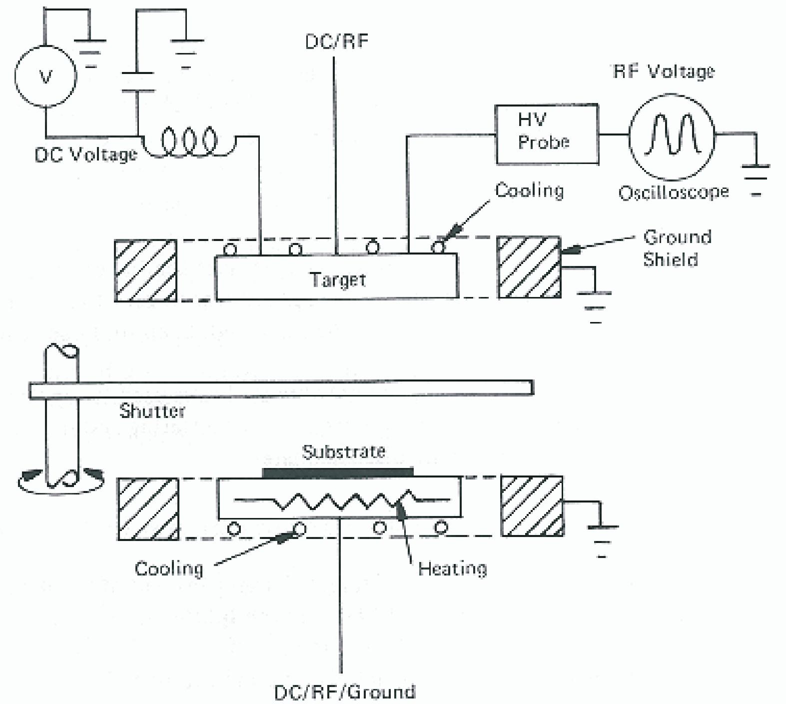
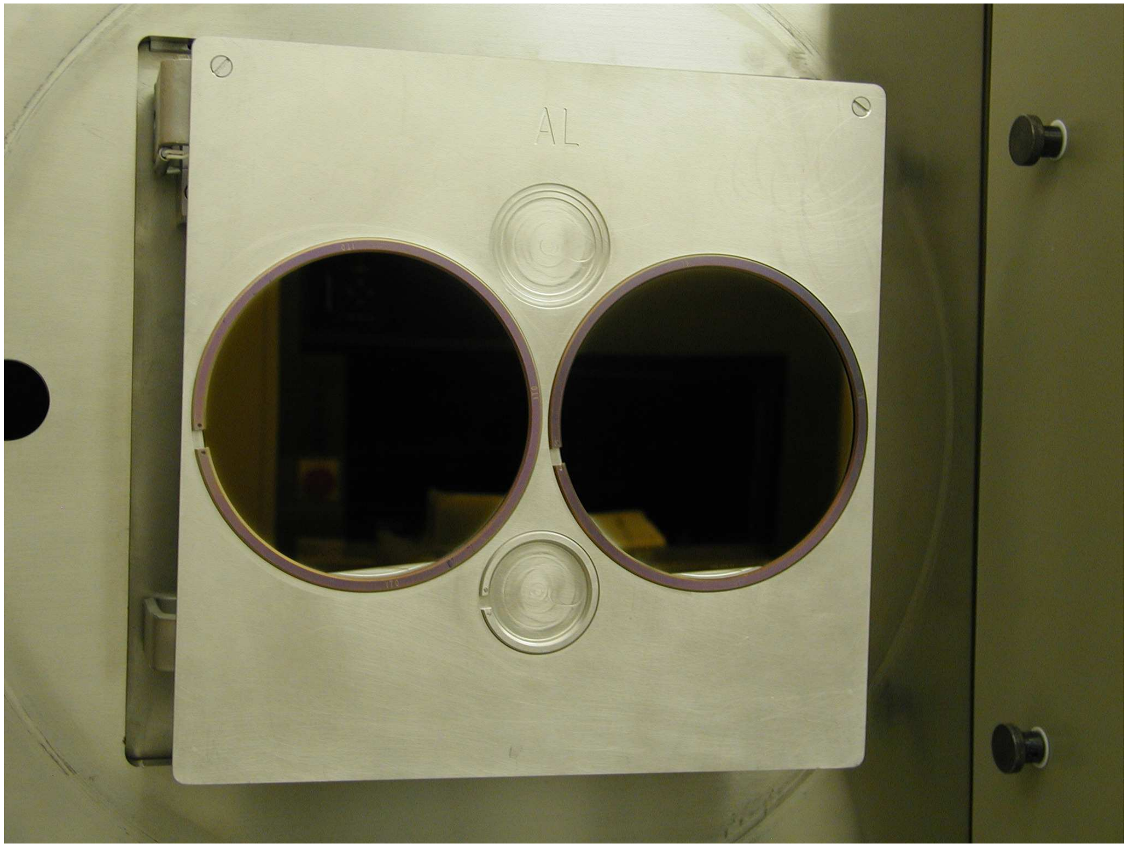


Figure 6-12. Schematic of a sputtering system showing ground shields, shutter, electrode cooling and heating, rf and dc voltage measurement

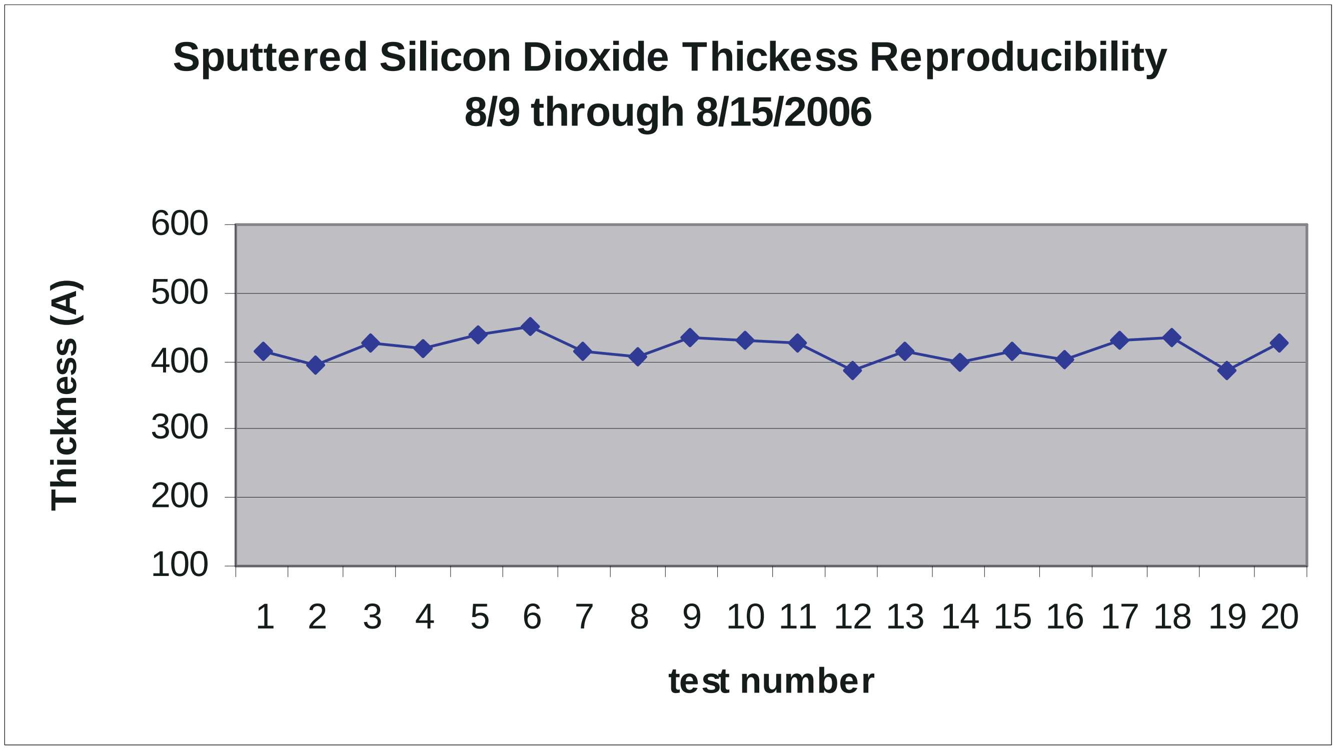
Schematic view of sputtering system

MSL – Sputter deposition



Completed ITO depositon on two 150mm wafers

MSL – Sputter deposition



Specification AR coating = 400 A

20 run average = 417 A, reproducibility = +/- 7.5%

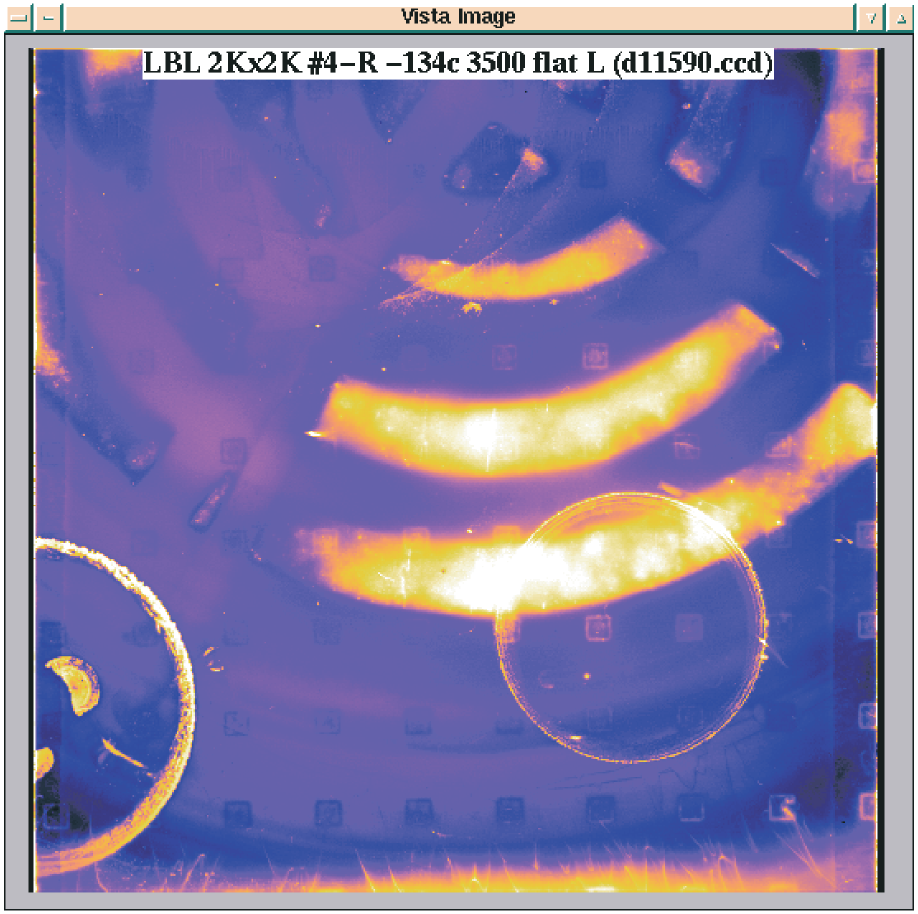
MSL – Measurements

Surfscan for measuring surface particles

Ellipsometer for measuring thin films

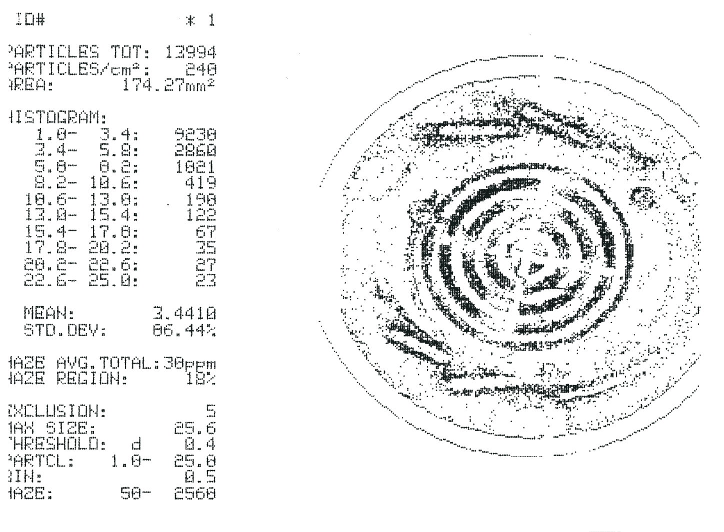
MSL – Measurements

Flat field image from MSL fabricated CCD showing effect of chuck contact on the wafer backside

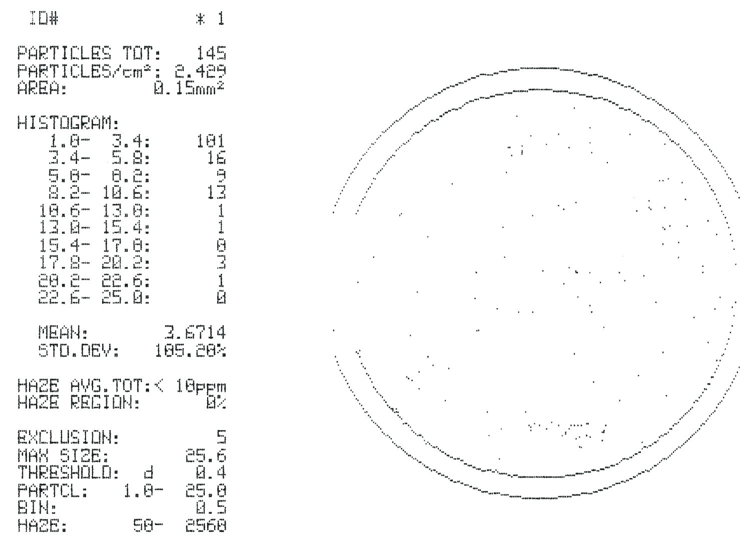


MSL – Measurements

Tencor Surfscan particle counter



Wafer surface particle map



Same wafer after scrub

MSL – Current work

- B.M. “production” CCD lots for Fermilab Dark Energy survey – 70 CCD commitment
- Continued iterations on the SNAP CCD design
- P-type pixel detectors for ALS application (Tindall/Denes)

MSL – Future plans

Device projects

- Continued support of CCD requirements for SNAP including possible final build
- X-ray detecting CCD (Holland/Denes)
- 4k x 4k CCD for the KECK telescope
- New materials?

MSL – Future plans

Facility enhancements

- Passivation deposition system – PECVD

- Automated microscope inspection station

Acknowledgements

- Graphics: S. Holland, D. Groom, N. Roe, C.Tindall, S. Wolf, B. Chapman
- MSL Staff: S. Holland, C. Tull, N. Wang, W.S. Hong, G. Wang, E. Johnson, C. Tindall, C. Tran
- Leadership: H. Spieler, M. Levi
- Support: Physics and Engineering Divisions